K.S.Rangasamy College of Technology

(Autonomous)

Curriculum & Syllabus

of

B.E. Electronics Engineering

(VLSI Design and Technology)

(For the batch admitted in 2025 – 2026)

R 2022

Accredited by NAAC with 'A++' Grade, Approved by AICTE
Affiliated to Anna University, Chennai

KSR Kalvi Nagar, Tiruchengode - 637 215
Namakkal District, Tamil Nadu, India

B.E. Electronics Engineering (VLSI Design and Technology)

Vision:

- To emerge as a distinguished center of academic excellence, offering exceptional education in Electronics Engineering, with a distinct focus on VLSI design and advanced research.

Mission:

- To nurture and develop professionals and technology leaders who uphold the highest standards of professional ethics in the realm of Electronics Engineering, with a focused specialization in VLSI design.
- To address the evolving needs of society by pushing the boundaries of disciplinary and multidisciplinary research in the field of Electronics Engineering, with our specialized focus on VLSI design.

PEOs:

PEO1: To empower graduates with the skills and knowledge necessary to achieve successful technical and professional career growth.

PEO2: To equip graduates with a profound understanding of the scientific, mathematical, and engineering fundamentals relevant to Electronics Engineering, with a specialized focus on VLSI design.

PEO3: To develop graduates who possess a commitment to lifelong learning, demonstrate creativity and innovation,and exhibit ethical and professional behavior, all while addressing the evolving needs of society.

PSOs :

Engineering Graduates will be able to:

PSO1: Develop graduates who are capable of solving complex engineering problems by applying their engineering knowledge in the fields of AI (Artificial Intelligence), IoT (Internet of Things), Signal Processing, VLSI design and related fields.

PSO2: Develop graduates who possess the capability to design system components and develop products that meet the specific needs of the industry and society in the field of Electronics Engineering, with a specialized focus on VLSI design.

PSO3: Develop graduates who possess essential interpersonal skills and attitudes required for ethical leadership and effective teamwork, including effective listening and communication, presentation skills, team building, and assertiveness.

PROGRAMME OUTCOMES (POs)

Engineering Graduates will be able to:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design /development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

MAPPING OF PEOs WITH POs and PSOs

Programme Educational Objectives	Programme Outcomes												Programme Specific Outcomes(PSO)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
PEO1	3	3	3	3	3	2	2	3	3	3	2	3	3	3	2
PEO2	3	3	3	3	3	3	3	3	3	3	3	3	3	3	2
PEO3	2	2	2	2	2	3	2	3	3	3	2	3	3	3	3

Contributions: 1- low, 2- medium, 3- high

MAPPING: Electronics Engineering (VLSI Design and Technology) (UG)

YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
I	I	60 EN 001	Professional English I	-	-	-	-	-	-	-	2	3	3	2	3
		60 MA 001	Matrices and Calculus	3	2	-	-	2	-	-	-	-	-	-	-
		60 PH 003	Physics for Electrical Engineering	3	-	-	-	-	-	-	-	-	2	-	-
		60 CS 001	C Programming	3	3	3	-	3	-	-	-	2	2	-	2
		60 ME 005	Foundation of Mechanical Engineering	3	3	-	-	-	-	-	2	3	3	-	-
		60 MY 001	Environmental Studies and Climate Change	3	2	-	-	3	2.7	2.8	2	-	-	-	2
		61 GE 001	Heritage of Tamils / தமிழர்மரபு	2	-	-	-	-	1.5	1	2.4	2	2	-	1.8
		60 CS 0P1	C Programming Laboratory	3	3	3	-	3	-	-	-	2	2	-	2
		61 ME 0P1	Fabrication and Reverse Engineering Laboratory	3	2	3			2	2	-	3	-	-	3
	II	60 EN 002	Professional English II	-	-	-	-	-	-	-	2	3	3	2	3
		60 MA 003	Integrals, Partial Differential Equations and Laplace Transform	3	3	-	-	2	-	-	-	-	-	-	-
		60 CH 003	Chemistry for Electronic Engineering	3	2.6	-	-	-	-	-	-	-	-	-	-
		60 ME 002	Engineering Graphics	3	2.8	3	-	3	-	-	3		-	-	-
		60 EV 201	Electronic Devices	3	2.6			3	-	-	3	3	3	-	3
		60 GE 002	Tamils and Technology / தமிழரும்தொழில்நுட்பமும்	3	-	-	-	3	2	2.8	3	2.5	2.2	-	3
		60 CP 0P2	Engineering Physics and Chemistry Laboratory	3	-	-	-	-	-	-	-	2		-	-
		60 EV 2P1	Electronic Devices Laboratory	3	3	-	-	3	3	-	3	3	3	-	3
		60 CG 0P1	Career Skill Development – I	-	-	-	-	-	-	-	2	3	3	2	3

YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
II	III	60 MA 009	Linear Algebra and Numerical Methods	3	2	-	-	2	-	-	-	-	-	-	-
		60 CS 002	Data Structures and Algorithms	3	3	2	2.6	2	2	2	2.4	2.6	2	-	2
		60 EV 301	Electronic Circuits	3	3	3	-	3	-	-	3	3	3	-	3
		60 EV 302	Circuit Analysis	3	3	-	-	2.6	-	-	-	3	3	-	2

Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

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		60 EV 303	Digital System Design	2.8	2.8	3	-	3	-	-	3	3	3	-	-
		60 MY 002	Universal Human Values	-	-	-	-	-	3	3	3	2.8	3	2	3
		60 EV 3P1	Analog and Digital Electronics Laboratory	2.8	2.8	3	-	2.6	-	-	-	3	3	-	3
		61 CS 0P2	Data Structures and Algorithms Laboratory	3	3	2	2.7	2	2	2	3	2.6	2	-	2
		60 CG 0P2	Career Skill Development – II	-	-	-	-	-	-	-	2	3	3	2	3
	IV	60 CG 0P6	Internship	-	-	-	-	-	-	-	-	-	-	-	-
		60 MA 016	Probability and Inferential Statistics	3	2	-	-	2	-	-	-	-	-	-	-
		61 EV 401	Signals and Systems	3	3	-	-	2	2	-	-	3	3	-	-
		60 EV 402	Linear Integrated Circuits	2.6	2.8	3	3	3	-	-	3	3	3	-	3
		60 EV 403	Electromagnetic Waves	3	3	3	-	-	-	-	3	3	3	-	3
		60 EV 404	Computer Architecture and Microcontrollers	3	3	3	3	-	-	-	3	3	3	-	3
		60 OE L1*	Open Elective I	-	-	-	-	-	-	-	-	-	-	-	-
		60 EV 4P1	Linear Integrated Circuits Laboratory	3	3	3	-	3	2.8	-	-	3	3	-	3
		60 EV 4P2	Microcontrollers Laboratory	3	3	3	2.8	3	-	-	3	3	3	-	3
		60 CG 0P3	Career Skill Development – III	2.6	2.6	2.6	2.8	-	2.4	-	-	-	2	-	3
		60 CG 0P6	Internship	-	-	-	-	-	-	-	-	-	-	-	-

YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
III	V	60 EV 501	Control Systems Engineering	3	3	3	-	2	-	-	-	3	3	-	-
		60 EV 502	VLSI and Chip Design	3	3	-	-	3	-	-	3	3	3	-	3
		60 EV 503	Digital Signal Processing	3	3	3	-	3	-	-	-	3	-	-	3
		60 EV 504	Machine Learning in VLSI System Design	3	2.6	2	2	2.2	-	-	-	-	-	-	-
		60 EV E1*	Professioanl Elective I	-	-	-	-	-	-	-	-	-	-	-	-
		60 OE L2*	Open Elective II	-	-	-	-	-	-	-	-	-	-	-	-
		60 MY 003	Startups and Entrepreneurship	2.8	2.6	3	2.4	2.2	2.5	1.7	1.7	1.3	2	2.2	2.4
		60 EV 5P1	VLSI Laboratory	3	3	-	-	3	-	-	3	3	3	-	3
		60 EV 5P2	Signal Processing Laboratory	3	3	3	-	3	-	-	3	3	3	-	3
		60 EV 5P3	Design Thinking and Innovation Laboratory	3	3	2.8	3	-	-	-	3	3	3	-	3
		60 CG 0P4	Career Skill Development IV	2.6	2.6	2.6	2.8	-	2.4	-	-	-	2	3	3
	VI	60 EV 601	Embedded Systems	3	3	2.8	3	3	-	-	3	3	3	-	3
		60 EV 602	Testing of VLSI Circuits	3	3	3	3	3	-	-	3	3	3	-	3
		60 EV 603	ASIC Design	3	2.8	2	2	2.8	-	-	3	3	3	-	3
		60 EV 604	Analog and Digital Communication	3	3	3	3	3	-	-	-	-	-	-	-
		60 EV E2*	Professioanl Elective II	-	-	-	-	-	-	-	-	-	-	-	-
		60 OE L3*	Open Elective III	-	-	-	-	-	-	-	-	-	-	-	-
		60 MY 004	Disaster Management	1	1	-	-	1	1.6	1.5	-	-	-	-	-
		60 EV 6P1	VLSI Verification and Testing Laboratory	3	3	3	3	3	-	-	3	3	3	-	3
		60 EV 6P2	Embedded Systems Laboratory	3	3	3	3	3	-	-	3	3	3	3	3
		60 EV 6P3	Design Thinking and Product Development Laboratory	-	-	-	-	-	-	-	-	-	-	-	-
		60 CG 0P5	Comprehension Test	3	3	2	2	-	-	-	-	1	2	2	3
		60 CG 0P6	Internship	-	-	-	-	-	-	-	-	-	-	-	-

Passed in BoS Meeting held on 20/12/2025
Approved in Academic Council Meeting held on 03/01/2026

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YEAR	SEM	COURSE CODE	COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
IV	VII	60 EV 701	Introduction to Microfabrication	3	3	3	2.6	2.2	-	-	1.8	-	-	-	1.8
		60 EV 702	Verification Methodologies and Bus Architectures	3	3	3	3	3	-	-	3	3	3	-	3
		60 EV 703	Electronic Packaging	3	3	3	-	3	-	-	-	3	-	-	3
		60 EV E3*	Professional Elective III	-	-	-	-	-	-	-	-	-	-	-	-
		60 EV E4*	Professional Elective IV	-	-	-	-	-	-	-	-	-	-	-	-
		60 AB 00*	NCC\NSS\NSO\YRC\RRC\Yoga\Fine Arts%	-	-	-	-	-	-	-	-	-	-	-	-
		60 AC 001	Research Skill Development	2	2	2	2	3	2	2	3	3	3	-	3
		60 EV 7P1	Microfabrication Laboratory	3	3	-	-	3	-	-	3	3	3	-	3
		60 EV 7P2	Project Work Phase - I	3	3	3	3	3	3	3	3	3	3	3	3
		60 CG 0P6	Internship												
	VIII	60 EV E5*	Professional Elective V	-	-	-	-	-	-	-	-	-	-	-	-
		60 EV 8P1	Project Work Phase - II	3	3	3	3	3	3	3	3	3	3	3	3
		60 CG 0P6	Internship	-	-	-	-	-	-	-	-	-	-	-	-

K.S. RANGASAMY COLLEGE OF TECHNOLOGY

Credit Distribution for B.E Electronics Engineering (VLSI Design and Technology) Programme – 2025 - 2026 Batch

S.No.	Category	Credits Per Semester								Total Credits	Percentage %
		I	II	III	IV	V	VI	VII	VIII		
1.	HS	2	2	-	-	-	-	-	-	**04**	**2.50**
2.	BS	7	9	4	4	-	-	-	-	**24**	**14.80**
3.	ES	10	4	3	-	-	-	-	-	**17**	**10.50**
4.	PC	-	5	14	16	18	18	12	-	**83**	**51.23**
5.	PE	-	-	-	-	3	3	6	3	**15**	**9.25**
6.	OE	-	-	-	3	3	3	-	-	**9**	**5.55**
7.	CG	-	-	-	-	-	-	2	8	**10**	**6.17**
8.	MC	-	-	-	-	-	-	-	-	**-**	**-**
9.	AC	-	-	-	-	-	-	-	-	**-**	**-**
10.	GE	-	-	-	-	-	-	-	-	**-**	**-**
Total		**19**	**20**	**21**	**23**	**24**	**24**	**20**	**11**	**162**	**100**

HS - HUMANITIES AND SOCIAL SCIENCES
BS - BASIC SCIENCE COURSES
ES - ENGINEERING SCIENCE COURSES
PC - PROFESSIONAL CORE COURSES
PE - PROFESSIONAL ELECTIVE COURSES
OE - OPEN ELECTIVES
CG - CAREER GUIDANCE COURSES
MC - MANDATORY COURSES
AC - AUDIT COURSES
GE - GENERAL ELECTIVE COURSES

- Open Electives are courses offered by different departments that do not have any prerequisites and could be of interest to students of any branch.

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HUMANITIES AND SOCIAL SCIENCES (HS)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EN 001	Professional English I	HS	3	1	0	2	2	Basic knowledge of reading and writing in English
2.	60 EN 002	Professional English II	HS	3	1	0	2	2	Basic knowledge of reading and writing in English and should have completed Professional English I.
3.	60 AB 001	National Cadet Corps (Air wing)	HS	4	2	0	2	3	NIL
4.	60 AB 002	National Cadet Corps (Army Wing)	HS	4	2	0	2	3	NIL

BASIC SCIENCE (BS)

S.No	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 MA 001	Matrices and Calculus	BS	5	3	1	0	4	NIL
2.	60 PH 003	Physics for Electrical Engineering	BS	3	3	0	0	3	NIL
3.	60 MA 003	Integrals, Partial Differential Equations and Laplace Transform	BS	5	3	1	0	4	NIL
4.	60 CH 003	Chemistry for Electronic Engineering	BS	3	3	0	0	3	NIL
5.	60 CP 0P2	Engineering Physics and Chemistry Laboratory	BS	4	0	0	4	2	NIL
6.	60 MA 009	Linear Algebra and Numerical Methods	BS	5	3	1	0	4	NIL
7.	60 MA 016	Probability and Inferential Statistics	BS	5	3	1	0	4	NIL

ENGINEERING SCIENCES (ES)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 CS 001	C Programming	ES	3	3	0	0	3	NIL
2.	60 ME 005	Foundation of Mechanical Engineering	ES	3	3	0	0	3	NIL
3.	60 CS 0P1	C Programming Laboratory	ES	4	0	0	4	2	NIL
4.	61 ME 0P1	Fabrication and Reverse Engineering Laboratory	ES	4	0	0	4	2	NIL
5.	60 ME 002	Engineering Graphics	ES	6	2	0	4	4	NIL

PROFESSIONAL CORE (PC)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV 201	Electronic Devices	PC	3	3	0	0	3	NIL
2.	60 EV 2P1	Electronic Devices Laboratory	PC	4	0	0	4	2	NIL

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3.	60 EV301	Electronic Circuits	PC	3	3	0	0	3	Electronic Devices
4.	60 EV302	Circuit Analysis	PC	6	2	1	2	4	NIL
5.	60 EV303	Digital System Design	PC	4	2	1	0	3	NIL
6.	60 EV 3P1	Analog and Digital Electronics Laboratory	PC	4	0	0	4	2	Electronic Devices Laboratory
7.	61 EV 401	Signals and Systems	PC	4	2	1	0	3	Integrals, Partial Differential Equations and Laplace transform
8.	60 EV 402	Linear Integrated Circuits	PC	3	3	0	0	3	Electronic Circuits
9.	60 EV 403	Electromagnetic Waves	PC	4	2	1	0	3	NIL
10.	60 EV 404	Computer Architecture and Microcontrollers	PC	3	3	0	0	3	Digital System Design
11.	60 EV 4P1	Linear Integrated Circuits Laboratory	PC	4	0	0	4	2	Electronic Circuits
12.	60 EV 4P2	Microcontrollers Laboratory	PC	4	0	0	4	2	Digital System Design
13.	60 EV 501	Control Systems Engineering	PC	5	3	1	0	4	Integrals and Partial Differential Equations
14.	60 EV 502	VLSI and Chip Design	PC	3	3	0	0	3	Digital System Design
15.	60 EV 503	Digital Signal Processing	PC	5	3	1	0	4	Signals and Systems
16.	60 EV 504	Machine Learning in VLSI System Design	PC	4	2	0	2	3	Neural Networks
17.	60 EV 505	Analog and Digital Communication	PC	5	3	1	0	4	Signals and Systems
18.	60 EV 5P1	VLSI Laboratory	PC	4	0	0	4	2	Digital System Design
19.	60 EV 5P2	Signal Processing Laboratory	PC	4	0	0	4	2	Digital Signal Processing
20.	60 EV 601	Embedded Systems	PC	3	3	0	0	3	Microprocessors and Microcontrollers
21.	60 EV 602	Testing of VLSI Circuits	PC	3	3	0	0	3	Digital System Design
22.	60 EV 603	ASIC Design	PC	5	3	0	2	4	VLSI and Chip design
23.	60 EV 604	Analog and Digital Communication	PC	5	3	0	2	4	Signals and Systems
24.	60 EV 6P1	VLSI Verification and Testing Laboratory	PC	4	0	0	4	2	Testing of VLSI Circuits
25.	60 EV 6P2	Embedded Systems Laboratory	PC	4	0	0	4	2	Microprocessors and Microcontrollers
26.	60 EV 701	Introduction to Microfabrication	PC	3	3	0	0	3	Basics of Physics&Chemistry, Devices& Circuit
27.	60 EV 702	Verification Methodologies and Bus Architectures	PC	5	3	0	2	4	Nil
28.	60 EV 703	Electronic Packaging	PC	3	3	0	0	3	Electronic Circuits and Embedded Systems
29.	60 EV 7P1	Microfabrication Laboratory	PC	4	0	0	4	2	Basic Programming & Electron Devices & Circuits

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PROFESSIONAL ELECTIVES (PE)

SEMESTER V, PROFESSIONAL ELECTIVE I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E11	Solid State Electronic Devices	PE	3	3	0	0	3	Electronic Devices
2.	60 EV E12	Analog VLSI Design	PE	3	3	0	0	3	Digital Design
3.	60 EV E13	ASIC synthesis and STA	PE	3	3	0	0	3	Digital Design, Electronics Fundamental and CMOS Design
4.	60 EV E14	HDL programming	PE	3	3	0	0	3	Digital Logic Circuits
5.	60 EV E15	FPGA Design	PE	3	3	0	0	3	Digital system design
6.	60 EV E16	Data science	PE	3	3	0	0	3	Nil

SEMESTER VI, PROFESSIONAL ELECTIVE II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E21	Semiconductor Equipment Design and Technology	PE	3	3	0	0	3	Electronic Devices
2.	60 EV E22	System Verilog	PE	3	3	0	0	3	Verilog HDL
3.	60 EV E23	Advanced Embedded Computing	PE	3	3	0	0	3	Microprocessors and Microcontrollers
4.	60 EV E24	VLSI Technology	PE	3	3	0	0	3	Digital Systems
5.	60 EV E25	Physical design of VLSI	PE	3	3	0	0	3	Digital Design, Electronics Fundamental and CMOS Design
6.	60 EV E26	Digital image Processing	PE	3	3	0	0	3	Nil

SEMESTER VII, PROFESSIONAL ELECTIVE III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E31	Low Power VLSI Design	PE	4	2	0	2	3	Electronic Circuit, VLSI Design
2.	60 EV E32	VLSI Signal Processing	PE	4	2	0	2	3	Signals and Systems, Digital Signal Processing
3.	60 EV E33	Scripting languages for VLSI design automation	PE	4	2	0	2	3	Nil
4.	60 EV E34	System On Chip	PE	4	2	0	2	3	Nil
5.	60 EV E35	Mixed Signal Design	PE	4	2	0	2	3	Basics of HDL and Analog circuits
6.	60 EV E36	Artificial Intelligence	PE	4	2	0	2	3	Nil

SEMESTER VII, PROFESSIONAL ELECTIVE IV

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E41	Nano Technology	PE	3	3	0	0	3	Nil
2.	60 EV E42	Analog IC Design	PE	3	3	0	0	3	Electronic Devices&Circuit

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3.	60 EV E43	Memory Design and Testing	PE	3	3	0	0	3	Digital System Design
4.	60 EV E44	Network on Chip	PE	3	3	0	0	3	Nil
5.	60 EV E45	IP based VLSI Design	PE	3	3	0	0	3	Nil
6.	60 EV E46	Computer Vision: Algorithms and Applications	PE	3	3	0	0	3	Nil

SEMESTER VIII, PROFESSIONAL ELECTIVE V

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E51	RTL Design and Synthesis	PE	3	3	0	0	3	Digital Logic Design
2.	60 EV E52	Algorithms for VLSI Design Automation	PE	3	3	0	0	3	Digital Logic Design, Data Structures and Algorithms
3.	60 EV E53	DSP structures for VLSI	PE	3	3	0	0	3	Digital Signal Processing
4.	60 EV E54	RFIC Design	PE	3	3	0	0	3	Electronic Circuits
5.	60 EV E55	Micro Electro Mechanical Systems	PE	3	3	0	0	3	Nil
6.	60 EV E56	Deep Learning	PE	3	3	0	0	3	Machine Learning Techniques

Any of the above six elective courses shall be opted for honours degree.

AUDIT COURSES (AC)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 AC 001	Research Skill Development	AC	1	1	0	0	0	Nil

MANDATORY COURSES (MC)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 MY 001	Environmental Studies and Climate Change	MC	2	2	0	0	0	Nil
2.	60 MY 002	Universal Human Values	MC	4	3	0	0	3	Nil
3.	60 MY 003	Startups and Entrepreneurship	MC	2	2	0	0	2*	Basic Konwlege of Reading and Writing in English
4.	60 MY 004	Disaster Management	MC	2	0	0	0	0	Nil

GENERAL ELECTIVE COURSES (GE)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 GE 001	Heritage of Tamils / தமிழர்மரபு	GE	1	1	0	0	1*	Nil
2.	60 GE 002	Tamils and Technology / தமிழரும்தொழில்நுட்பமும்	GE	1	1	0	0	1*	Nil

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OPEN ELECTIVES I / II / III (OE)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV E24/ 60 EV L01	VLSI Technology	OE	3	3	0	0	3	Digital Systems
2.	60 EV E15/ 60 EV L02	FPGA Design	OE	3	3	0	0	3	Digital System Design
3.	60 EV E55/ 60 EV L03	Micro Electro Mechanical Systems	OE	3	3	0	0	3	Nil

INTEGRATED COURSES

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
1.	60 EV 302	Circuit Analysis	PC	5	2	1	2	4	Nil
2.	60 EV 504	Machine Learning in VLSI System Design	PC	4	2	0	2	3	Neural Networks
3.	60 EV 603	ASIC Design	PC	5	3	0	2	4	VLSI and Chip Design
4.	60 EV E3*	Professional Elective III	PE	4	2	0	2	3	-
5.	60 EV 702	Verification Methodologies and Bus Architectures	PC	5	3	0	2	4	Nil

CAREER ENHANCEMENT COURSES (CG)

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C	Prerequisite
6.	60 CG 0P1	Career Skill Development – I	CG	2	0	0	2	1*	Nil
7.	60 CG 0P2	Career Skill Development – II	CG	2	0	0	2	1*	Nil
8.	60 CG 0P3	Career Skill Development – III	CG	2	0	0	2	1*	Nil
9.	60 CG 0P4	Career Skill Development – IV	CG	2	0	0	2	1*	Nil
10.	60 CG 0P5	Comprehension Test	CG	2	0	0	2	1*	Nil
11.	60 EV 7P2	Project Work Phase - I	CG	4	0	0	4	2	Nil
12.	60 EV 8P1	Project Work Phase - II	CG	16	0	0	16	8	Nil
13.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$	Nil

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Approved in Academic Council Meeting held on 19/07/2025

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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE -637215
(An Autonomous Institution affiliated to Anna University)
COURSES OF STUDY
(For the candidates admitted in 2025-2026)
SEMESTER I

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
		Induction Programme	-	-	-	-	-	-
THEORY								
1.	60 EN 001	Professional English I	HS	3	1	0	2	2
2.	60 MA 001	Matrices and Calculus	BS	5	3	1	0	4
3.	60 PH 003	Physics for Electrical Engineering	BS	3	3	0	0	3
4.	60 CS 001	C Programming	ES	3	3	0	0	3
5.	60 ME 005	Foundation of Mechanical Engineering	ES	3	3	0	0	3
6.	60 MY 001	Environmental Studies and Climate Change	MC	2	2	0	0	0
7.	61 GE 001	Heritage of Tamils / தமிழர்மரபு	GE	1	1	0	0	1*
PRACTICALS								
8.	60 CS 0P1	C Programming Laboratory	ES	4	0	0	4	2
9.	61 ME 0P1	Fabrication and Reverse Engineering Laboratory	ES	4	0	0	4	2
			Total	**28**	**16**	**1**	**10**	**19**

I to VII semester

- NCC% - Course can be waived with 3 credits in VII semester or offered as extra credits
- NSS/NSO/YRC/RRC/Fine Arts% - 3 credits not accounted for CGPA calculation
- Career Skill Development (CSD)* - Additional credits not accounted for CGPA calculation

I to VIII semester

- Internship$ - Additional 3 credits not accounted for CGPA calculation based on duration
- Heritage of Tamils* - Additional 1 credit not accounted for CGPA

SEMESTER II

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 EN 002	Professional English II	HS	3	1	0	2	2
2.	60 MA 003	Integrals, Partial Differential Equations and Laplace Transform	BS	5	3	1	0	4
3.	60 CH 003	Chemistry for Electronic Engineering	BS	3	3	0	0	3
4.	60 ME 002	Engineering Graphics	ES	6	2	0	4	4
5.	60 EV 201	Electronic Devices	PC	3	3	0	0	3

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6.	60 GE 002	Tamils and Technology / தமிழரும்தொழில்நுட்பமும்	GE	1	1	0	0	1*
PRACTICALS								
7.	60 CP 0P2	Engineering Physics and Chemistry Laboratory	BS	4	0	0	4	2
8.	60 EV 2P1	Electronic Devices Laboratory	PC	4	0	0	4	2
9.	60 CG 0P1	Career Skill Development I	CG	2	0	0	2	1*
			Total	**31**	**13**	**1**	**16**	**20**

- Tamils and Technology* - Additional 1 credit not accounted for CGPA calculation.

SEMESTER III

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 MA 009	Linear Algebra and Numerical Methods	BS	5	3	1	0	4
2.	60 CS 002	Data Structures and Algorithms	ES	3	3	0	0	3
3.	60 EV 301	Electronic Circuits	PC	3	3	0	0	3
4.	60 EV 302	Circuit Analysis	PC	6	2	1	2	4
5.	60 EV 303	Digital System Design	PC	4	2	1	0	3
6.	60 MY 002	Universal Human Values	MC	3	3	0	0	3#
PRACTICALS								
7.	60 EV 3P1	Analog and Digital Electronics Laboratory	PC	4	0	0	4	2
8.	61 CS 0P2	Data Structures and Algorithms Laboratory	PC	4	0	0	4	2
9.	60 CG 0P2	Career Skill Development II	CG	2	0	0	2	1*
10.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**34**	**16**	**3**	**12**	**21**

- UHV# - Additional 3 credits not accounted for CGPA calculation

SEMESTER IV

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 MA 016	Probability and Inferential Statistics	BS	5	3	1	0	4
2.	61 EV 401	Signals and Systems	PC	4	2	1	0	3
3.	60 EV 402	Linear Integrated Circuits	PC	3	3	0	0	3
4.	60 EV 403	Electromagnetic Waves	PC	4	2	1	0	3
5.	60 EV 404	Computer Architecture and Microcontrollers	PC	3	3	0	0	3
6.	60 OE L1*	Open Elective I	OE	3	3	0	0	3

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PRACTICALS								
7.	60 EV 4P1	Linear Integrated Circuits Laboratory	PC	4	0	0	4	2
8.	60 EV 4P2	Microcontrollers Laboratory	PC	4	0	0	4	2
9.	60 CG 0P3	Career Skill Development III	CG	2	0	0	2	1*
10.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**32**	**16**	**3**	**10**	**23**

SEMESTER V

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 EV 501	Control Systems Engineering	PC	5	3	1	0	4
2.	60 EV 502	VLSI and Chip Design	PC	3	3	0	0	3
3.	60 EV 503	Digital Signal Processing	PC	5	3	1	0	4
4.	60 EV 504	Machine Learning in VLSI System Design	PC	4	2	0	2	3
5.	60 EV E1*	Professional Elective I	PE	3	3	0	0	3
6.	60 OE L2*	Open Elective II	OE	3	3	0	0	3
7.	60 MY 003	Startups and Entrepreneurship	MC	2	2	0	0	2##
PRACTICALS								
8.	60 EV 5P1	VLSI Laboratory	PC	3	0	0	3	1.5
9.	60 EV 5P2	Signal Processing Laboratory	PC	3	0	0	3	1.5
10.	60 EV 5P3	Design Thinking and Innovation Laboratory	CG	2	0	0	2	1
11.	60 CG 0P4	Career Skill Development IV	CG	2	0	0	2	1*
12.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**35**	**18**	**2**	**12**	**24**

- Startups and Entrepreneurship## - Additional 2 credit not accounted for CGPA calculation

SEMESTER VI

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 EV 601	Embedded Systems	PC	3	3	0	0	3
2.	60 EV 602	Testing of VLSI Circuits	PC	3	3	0	0	3
3.	60 EV 603	ASIC Design	PC	5	3	0	2	4
4.	60 EV 604	Analog and Digital Communication	PC	5	3	1	0	4

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5.	60 EV E2*	Professional Elective II	PE	3	3	0	0	3
6.	60 OE L3*	Open Elective III	OE	3	3	0	0	3
7.	60 MY 004	Disaster Management	MC	2	0	0	0	0
PRACTICALS								
8.	60 EV 6P1	VLSI Verification and Testing Laboratory	PC	3	0	0	3	1.5
9.	60 EV 6P2	Embedded Systems Laboratory	PC	3	0	0	3	1.5
10.	60 EV 6P3	Design Thinking and Product Development Laboratory	CG	2	0	0	2	1
11.	60 CG 0P5	Comprehension Test	CG	2	0	0	2	1*
12.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**34**	**18**	**1**	**12**	**24**

- Comprehension Test* - Additional 1 credit not accounted for CGPA calculation

SEMESTER VII

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 EV 701	Introduction to Microfabrication	PC	3	3	0	0	3
2.	60 EV 702	Verification Methodologies and Bus Architectures	PC	5	3	0	2	4
3.	60 EV 703	Electronic Packaging	PC	3	3	0	0	3
4.	60 EV E3*	Professional Elective III	PE	4	2	0	2	3
5.	60 EV E4*	Professional Elective IV	OE	3	3	0	0	3
6.	60 AB 00*	NCC\NSS\NSO\YRC\RRC\Yoga\Fine Arts	HS	4	2	0	2	3*
7.	60 AC 001	Research Skill Development	AC	1	1	0	0	0
PRACTICALS								
8.	60 EV 7P1	Microfabrication Laboratory	PC	4	0	0	4	2
9.	60 EV 7P2	Project Work Phase - I	CG	4	0	0	4	2
10.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**27**	**15**	**0**	**12**	**20**

NCC% - Course can be waived with 3 credits in VII semester or offered as extra 3 credits
NSS/NSO/YRC/RRC/Fine Arts% - Additional 3 credits not accounted for CGPA calculation

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SEMESTER VIII

S.No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1.	60 EV E5*	Professional Elective V	PE	3	3	0	0	3
PRACTICALS								
2.	60 EV 8P1	Project Work Phase - II	CG	16	0	0	16	8
3.	60 CG 0P6	Internship	CG	0	0	0	0	1/2 /3$
			Total	**19**	**3**	**0**	**16**	**11**

TOTAL NUMBER OF CREDITS TO BE EARNED FOR AWARD OF THE DEGREE = 162

Note: HS- Humanities and Social Sciences including Management Courses, BS- Basic Science Courses, ES-Engineering Science Courses, PE-Professional Core Courses, PE-Professional Elective Courses, GE-General Elective Courses, OE- Open Elective Courses, CG -Career Enhancement Course, MC- Mandatory Courses

L: Lecture
T: Tutorial
P: Practical

Note:
1 Hour Lecture is equivalent to 1 credit
2 Hours Tutorial is equivalent to 1 credit
2 Hours Practical is equivalent to1 credit

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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
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B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

FIRSTSEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EN 001	Professional English I	2	40	60	100	45	100
2.	60 MA 001	Matrices and Calculus	2	40	60	100	45	100
3.	60 PH 003	Physics for Electrical Engineering	2	40	60	100	45	100
4.	60 CS 001	C Programming	2	40	60	100	45	100
5.	60 ME 005	Foundation of Mechanical Engineering	2	40	60	100	45	100
6.	60 MY 001	Environmental Studies and Climate Change	2	100	-	100	-	100
7.	61 GE 001	Heritage of Tamils / தமிழர்மரபு	2	40	60	100	45	100
PRACTICAL								
8.	60 CS 0P1	C Programming Laboratory	3	60	40	100	45	100
9.	61 ME 0P1	Fabrication and Reverse Engineering Laboratory	3	60	40	100	45	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 marks for practical End Semester Examination.

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60 EN 001	Professional English I	Category	L	T	P	Credit
		HS	1	0	2	2

Objectives

- To help learners improve their vocabulary and to enable them to use words appropriately in different academic and professional contexts
- To help learners develop strategies that could be adopted while reading texts
- To help learners acquire the ability to speak effectively in English in real life and career related situations
- To equip students with effective speaking and listening skills in English
- To facilitate learners to enhance their writing skills with coherence and appropriate format effectively

Pre-requisites

- Basic Knowledge of Reading and Writing in English

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Compare and interpret complex academic texts	Understand
CO2	Recall the denotative and connotative meanings of technical texts	Remember
CO3	Interpret definitions, descriptions, narrations, and essays on various topics	Understand
CO4	Express fluently and accurately in formal and informal communicative contexts	Understand
CO5	Summarize their opinions effectively in both oral and written medium of communication	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO2	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO3	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO4	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO5	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
1- low, 2- medium, 3- high															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	50	80
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

Common to All Branches

60 EN 001 - Professional English I

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	1	0	2	45	2	40	60	100

Introduction to Fundamentals of Communication* **Listening:** General Information - Specific Details-Conversation - Introduction to Classmates - Audio - Video (Formal - Informal). **Speaking:** Self Introduction - Introducing A Friend - Conversation - Politeness Strategies. **Reading:** Reading Brochures (Technical Context), Telephone Messages - Social Media Messages Relevant to Technical Contexts and Emails. **Writing:** Writing Letters - Informal and Formal - Basics and Format Orientation **Language Focus:** Present Tenses - Word Formation (Affixes) - Synonyms, Antonyms and Contranyms - and Phrasal Verbs - Abbreviations - Acronyms (As Used in Technical Contexts).	[9]
Narration and Summation* **Listening:** Podcast, Anecdotes - Stories - Event Narration; Documentaries and Interviews with Celebrities. **Speaking:** Narrating Personal Experiences / Events; Interviewing a Celebrity; Reporting / And Summarizing of Documentaries / Podcasts/ Interviews. **Reading:** Biographies, Travelogues - Newspaper Reports - Excerpts from Literature - And Travel - Technical Blogs. **Writing:** Paragraph Writing - Short Report on An Event (Field Trip Etc.). **Language Focus:** Past Tenses and Prepositions - One-Word Substitution.	[9]
Description of A Process - Product* **Listening:** Listen to A Product and Process Descriptions; Advertisements about Products or Services. **Speaking:** Picture Description; Giving Instruction to Use the Product; Presenting a Product. **Reading:** Advertisements, Gadget Reviews and User Manuals. **Writing:** Definitions; Instructions; And Product - Process Description. **Language Focus:** Imperatives - Comparative Adjectives - Future Tenses. Homonyms - and Homophones - Discourse Markers (Connectives - Sequence Words).	[9]
Classification and Recommendations * **Listening:** TED Talks; Scientific Lectures and Educational Videos. **Speaking:** Small Talk; Mini Presentations. **Reading:** Newspaper Articles and Journal Reports. **Writing:** Note-Making / Note-Taking; Recommendations; Transferring Information from Non-Verbal (Chart, Graph Etc, To Verbal Mode). **Language Focus:** Articles; Pronouns - Possessive - Relative Pronouns; Subject-Verb Agreement; Collocations.	[9]
Expression* **Listening:** Debates/ Discussions; Different Viewpoints on an Issue; and Panel Discussions. **Speaking:** Group Discussions, Debates - Role Plays. **Reading:** Editorials; and Opinion Blogs. **Writing:** Essay Writing (Descriptive or Narrative). **Language Focus:** Punctuation; Compound Nouns; Simple, Compound - Complex Sentences. Cause - Effect Expressions.	[9]
Total Hours:	**45**

Text Book(s):

1.	"English for Engineers & Technologists", Orient Blackswan Private Ltd. Department of English, Anna University, 2020.
2.	Norman Lewis, "Word Power Made Easy - The Complete Handbook for Building a Superior Vocabulary Book", Penguin Random House India, 2020.

Reference(s):

1.	Paul Emmerson and Nick Hamilton, "Five Minute Activities for Business English", Cambridge University Press, New York, 2005.
2.	Arthur Brookes and Peter Grundy," Beginning to Write: Writing Activities for Elementary and Intermediate Learners", Cambridge University Press, New York, 2003
3.	Michael McCarthy and Felicity O Dell, "English Vocabulary in Use: Upper Intermediate", Cambridge University Press, N.York, 2012
4.	Lakshmi Narayanan, "A Course Book on Technical English", Scitech Publications (India) Pvt. Ltd., 2020.

*SDG4: Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Introduction to Fundamentals of Communication**	
1.1	Listening for General Information and Specific Details	1
1.2	Self-Introduction & Narrating Personal Experiences	2
1.3	Reading Relevant to Technical Contexts and Emails	1
1.4	Writing Letters - Informal & Formal	2
1.5	Present Tenses	1
1.6	Synonyms, Antonyms and Contranyms, And Affixes	1
1.7	Phrasal Verbs; Abbreviations & Acronyms	1
2	**Narration and Summation**	
2.1	Listening to Podcasts, Documentaries and Interviews with Celebrities	1
2.2	Narrating Personal Experiences	1
2.3	Summarizing of Documentaries	1
2.4	Reading Travelogues, And Excerpts from Literature	1
2.5	Paragraph Writing	1
2.6	Short Report on An Event (Field Trip Etc.).	1
2.7	Past Tenses & Prepositions	2
2.8	One-Word Substitution	1
3	**Description of A Process / Product**	
3.1	Listen to A Product and Process Descriptions	1
3.2	Picture Description	1
3.3	Giving Instruction to Use the Product	1
3.4	Reading Advertisements, Gadget Reviews and User Manuals	1
3.5	Writing Definitions and Instructions	1
3.6	Future Tenses	1
3.7	Homonyms and Homophones	1
3.8	Imperatives	1
3.9	Comparative Adjectives, And Discourse Markers	1
4	**Classification and Recommendations**	
4.1	Listening to TED Talks and Educational Videos	1
4.2	Listening to Scientific Lectures	1
4.3	Small Talk and Mini Presentations	1
4.4	Reading Newspaper Articles and Journal Reports	1
4.5	Note-Making / Note-Taking & Recommendations	2
4.6	Transferring Information from Non-Verbal & Articles and Pronouns	2
4.7	Subject-Verb Agreement and Collocations	1
5	**Expression**	
5.1	Listening to Debates and Panel Discussions	1
5.2	Group Discussions	2
5.3	Role Plays	1
5.4	Reading Editorials and Opinion Blogs	1
5.5	Essay Writing (Descriptive or Narrative)	1
5.6	Punctuation and Cause - Effect Expressions	1
5.7	Compound Nouns	1

Course Designer(s)

1. Dr.A.Palaniappan - Palaniappan@Ksrct.ac.In

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60 MA 001	Matrices and Calculus	Category	L	T	P	Credit
		BS	3	1	0	4

Objectives

- To familiarize the basic concepts in Cayley-Hamilton theorem and orthogonal transformation
- To get exposed to the fundamentals of differentiation
- To acquire skills to understand the concepts involved in Jacobians and maxima and minima
- To solve various linear differential equations and method of variation of parameters
- To learn various techniques and methods in solving definite and indefinite integrals

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the concepts of Cayley-hamilton theorem and orthogonal transformation to the matrix	Apply
CO2	Apply the concepts of differentiation in solving various Engineering problems	Apply
CO3	Obtain Jacobians and maxima and minima of functions of two variables	Apply
CO4	Employ various methods in solving differential equations	Apply
CO5	Apply different techniques to evaluate definite and indefinite integrals	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO5	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-

3 - Strong;2 - Medium;1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	20
Apply	40	40	70
Analyze	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

Common to MECH, EE, ECE, EEE, CSE, MCT, CIVIL, IT, TXT, BT, FT, AI&DS, AI&ML

60 MA 001 – Matrices and Calculus

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	1	0	60	4	40	60	100

Matrices Characteristic equation – Eigen values and Eigen vectors of a real matrix – Properties of Eigen values and Eigen vectors – Cayley-Hamilton theorem – Orthogonal transformation of a symmetric matrix to diagonal form – Reduction of quadratic form to canonical form by an Orthogonal transformation – Nature of quadratic form – Applications: Stretching of an elastic membrane Hands-on: Matrix Operations – Addition, Multiplication, Transpose, Inverse and Rank	[9]
Differentiation Representation of functions – Limit of a function – Continuity – Derivatives – Differentiation rules (sum, product, quotient, chain rules) – Successive Differentiation – Leibnitz's theorem **–** Applications: Maxima and Minima of functions of one variable* Hands-on: Determine the solution of system of linear equations	[9]
Functions of Several Variables Partial differentiation – Homogeneous functions and Euler's theorem – Jacobians – Taylor's series for functions of two variables – Applications: Maxima and minima of functions of two variables – Constrained maxima and minima: Lagrange's Method of Undetermined Multipliers* Hands-on: Compute the Eigen values and Eigen vectors of a Matrix	[9]
Differential Equations Linear differential equations of second and higher order with constant coefficients – R.H.S is of the form $e^{\alpha x}$, $\sin \alpha x$, $\cos \alpha x$, x^n, $n > 0$ – Differential equations with variable coefficients: Cauchy's and Legendre's form of linear equations – Method of variation of parameters Hands-on: Solve the first and second order ordinary differential equations	[9]
Integration Definite and Indefinite integrals – Substitution rule – Techniques of Integration: Integration by parts, Integration of rational functions by partial fraction, Integration of irrational functions – Improper integrals – Applications: Hydrostatic force and pressure, moments and centres of mass Hands-on: Compute the Maxima and Minima of a function of one variable	[9]
Total Hours: 45 + 5 (Hands-on) + 10 (Tutorial):	**60**

Text Book(s):	
1.	Grewal B.S, "Higher Engineering Mathematics", 44th Edition, Khanna Publishers, Delhi, 2017.
2.	Kreyszig Erwin, "Advanced Engineering Mathematics", 10th Edition, John Wiley and Sons (Asia) Limited, New Delhi, 2016.
Reference(s):	
1.	Dass H.K, "Higher Engineering Mathematics", 3rd (Revised) Edition, S.Chand & Company Ltd, New Delhi, 2014.
2.	Veerarajan T, "Engineering Mathematics", for Semesters I & II, 1st Edition, Tata McGraw Hill Publishing Co., New Delhi, 2019.
3.	Kandasamy P, Thilagavathy K and Gunavathy K, "Engineering Mathematics – I", S.Chand & Company Ltd, New Delhi, 2017.
4.	Bali N P and Manish Goyal," A text book of Engineering Mathematics",10th Edition, Laxmi Publications (P) Ltd, 2016.

*SDG4: Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Matrices**	
1.1	Characteristic equation	1
1.2	Eigen values and Eigen vectors of a real matrix	1
1.3	Properties of Eigen values and Eigen vectors	1
1.4	Cayley-Hamilton theorem	1
1.5	Orthogonal transformation of a symmetric matrix to diagonal form	1
1.6	Nature of quadratic form	1
1.7	Reduction of quadratic form to canonical form by Orthogonal transformation	2
1.8	Stretching of an elastic membrane	1
1.9	Tutorial	2
1.10	Hands-on	1
2	**Differentiation**	
2.1	Representation of functions	1
2.2	Limit of a function and Continuity	1
2.3	Differentiation rules (sum, product, quotient, chain rules)	2
2.4	Successive differentiation	1
2.5	Leibnitz's theorem	2
2.6	Maxima and minima of functions of one variable	2
2.7	Tutorial	2
2.8	Hands-on	1
3	**Functions of Several Variables**	
3.1	Partial differentiation	1
3.2	Homogeneous functions and Euler's theorem	1
3.3	Jacobians	2
3.4	Taylor's series for functions of two variables	1
3.5	Maxima and minima of functions of two variables	2
3.6	Lagrange's Method of Undetermined Multipliers	2
3.7	Tutorial	2
3.8	Hands-on	1
4	**Differential Equations**	
4.1	Linear differential equations of second and higher order with constant co-efficient	1
4.2	R.H.S is of the form $e^{\alpha x},\ sin\,\alpha\, x,\ cos\,\alpha\, x,\ x^n, n > 0$	2
4.3	Differential equations with variable coefficients: Cauchy's form of linear equations	2
4.4	Differential equations with variable coefficients: Legendre's form of linear equations	2
4.5	Method of variation of parameters	2
4.6	Tutorial	2
4.7	Hands-on	1
5	**Integration**	
5.1	Definite and Indefinite integrals	2
5.2	Substitution rule	1
5.3	Techniques of Integration: Integration by parts	1
5.4	Integration of rational functions by partial fraction	1
5.5	Integration of irrational functions	1
5.6	Improper integrals	1
5.7	Hydrostatic force.	1
5.8	Pressure, moments and centres of mass.	1
5.9	Tutorial	2
5.10	Hands-on	1
	Total	**60**

Course Designer(s)

1. Dr.C.Chandran – Cchandran@ksrct.ac.In
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60 PH 003	Physics for Electrical Engineering (ECE, EE & EEE)	Category	L	T	P	Credit
		BS	3	0	0	3

Objectives

- To make the students to understand the basics of crystallography, crystal growth and its importance in semiconductor devices
- To enable the students in understanding the importance of quantum physics and its applications.
- To instil knowledge on physics of semiconductors, determination of charge carriers and device applications
- To understand the dielectric properties of materials including magnetic materials, applications of dielectrics and magnetic materials
- To introduce advanced materials and nano technology for various modern engineering applications

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Recognize the basics of crystallography, different crystal growth techniques and its applications	Understand
CO2	Utilize the fundamentals of quantum mechanics and apply to one dimensional motion of particles	Apply
CO3	Acquire knowledge on basics of semiconductor physics and its applications in various devices	Understand
CO4	Realize the knowledge on magnetic and dielectric properties of materials and their applications	Understand
CO5	Infer the properties of new engineering materials and nano materials for potential applications	Understand

Mapping with Programme Outcomes

Cos	Pos												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	-	-	-	-	-	-	2	-	2	-	-	-	-	-
CO2	3	-	-	-	-	-	-	2	-	2	-	-	-	-	-
CO3	3	-	-	-	-	-	-	2	-	2	-	-	-	-	-
CO4	3	-	-	-	-	-	-	2	-	2	-	-	-	-	-
CO5	3	-	-	-	-	-	-	2	-	2	-	-	-	-	-
1- Low, 2- Medium, 3- High															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	14	16
Understand	46	46	80
Apply	04	-	04
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Common to EEE, EE, ECE

60 PH 003 – Physics for Electrical Engineering

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Crystal Structure of Solids* Lattice – Unit Cell – Crystal Systems And Bravais Lattice – Miller Indices – D Spacing in Cubic Lattice – Calculation of Number of Atoms Per Unit Cell – Atomic Radius – Coordination Number – Packing Factor For HCP Structure - Production of Single Crystal Silicon By Melt Growth Techniques (Bridgman and Czochralski) – Basic Properties of Silicon Wafers – Wafer Orientation – Wafer Cleaning – Pattern Alignment – Imperfections in Crystals.	[9]
Quantum Mechanics* Black Body Radiation – Dual Nature of Light – De-Broglie Hypothesis – Properties of Matter Waves – Time-Dependent and Time Independent Schrodinger Equation for Wave Function – Applications: Particle in a Box (One Dimensional and Three Dimensional) – Physical Significance of Wave Function-Uncertainty Principle – Applications – Electron Microscope – Scanning Electron Microscope.	[9]
Semiconducting Materials Properties-Elemental and Compound Semiconductors – Carrier Concentration in Intrinsic and Extrinsic Semiconductors- Experimental Determinations of Resistivity of Semiconductor by Four Probe Method – Hall Coefficient-Experimental Determination of Hall Coefficient- Semiconductor Devices – P-N Junction Diode, **Solar Cell, Led****.	[9]
Magnetic and Dielectric Materials* Magnetic Materials: Origin of Magnetic Moment – Bohr Magnetron – Classification of Magnetic Materials –Domain Theory – Hysteresis – Soft and Hard Magnetic Materials – Applications – Giant Magneto Resistance (Gmr). Dielectric Materials: Polarization – Electronic, Ionic, Orientational and Space Charge – Frequency and Temperature Dependence of Polarization- Breakdown Mechanisms – Applications of Dielectrics in Capacitor and Transformer.	[9]
Advanced Materials and Nanotechnology* Advanced Materials: Metallic Glasses – Preparation, Properties and Applications – Shape Memory Alloys (SMA) – Characteristics, Properties of Niti Alloy Applications. Nano Technology: Properties- Top-Down Process: Ball Milling Method – Bottom-Up Process: Vapour Phase Deposition – Carbon Nano Tube (CNT): Properties, Preparation by Electric Arc Method – Application –Single Electron Phenomena and Single Electron Transistor (Set)	[9]
Total Hours:	**45**

Text Book(s):

1. Avadhanulu M. N., Kshirsagar P. G., Arun Murthy TVS, “A Text Book of Engineering Physics”, S Chand Publications, New Delhi, 2022.
2. Malik H. K., Singh A. K., “Engineering Physics”, McGraw Hill Education Private Limited, New Delhi. 2021.
3. Joshi D. R., “Engineering Physics”, McGraw Hill Education Private Limited, New Delhi. 2010.

Reference(s):

1. Pillai S.O., “A Textbook Of Engineering Physics”, New Age International (P) Limited, New Delhi, 2014.
2. Laud B. B., “Lasers and Non-Linear Optics”, New Age International Publications, New Delhi, 2015.
3. Palanisamy, P.K., “Physics of Materials”, Scitech Publications, Chennai. 2012.

* SDG 4- Quality Education

** SDG 7 – Sustainable and modern energy for all

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Crystal Structure of Solids**	
1.1	Lattice – Unit cell – crystal systems and Bravais lattice	1
1.2	Miller indices – d spacing in cubic lattice	1
1.3	Calculation of number of atoms per unit cell	1
1.4	Atomic radius – Coordination number – Packing factor for HCP structure	1
1.5	Production of single crystal silicon by melt growth techniques	1
1.6	(Bridgman and Czochralski)	1
1.7	Basic Properties of Silicon Wafers	1
1.8	Wafer orientation – wafer cleaning	1
1.9	Pattern alignment – imperfections in crystals	1
2.0	**Quantum Mechanics**	
2.1	Black body radiation	1
2.2	Dual nature of light – de-Broglie hypothesis	1
2.3	Properties of matter waves	1
2.4	Time-dependent and time independent Schrodinger equation for wave function	1
2.5	Applications: Particle in a box (one dimensional and three dimensional)	1
2.6	Physical significance of wave function-Uncertainty principle	1
2.7	Applications of Schrodinger equation	1
2.8	Electron microscope	1
2.9	Scanning electron microscope	1
3.0	**Semiconducting Materials**	
3.1	Properties of semiconductor	1
3.2	Elemental and Compound Semiconductors	1
3.3	Carrier Concentration in intrinsic and Extrinsic semiconductors	1
3.4	Experimental determinations of resistivity of semiconductor	1
3.5	Four probe method	1
3.6	Hall Coefficient	1
3.7	Experimental Determination of Hall Coefficient	1
3.8	Semiconductor devices – P-N Junction diode	1
3.9	Solar Cell, LED	1
4.0	**Magnetic and Dielectric Materials**	
4.1	Origin of magnetic moment – Bohr magnetron	1
4.2	Classification of magnetic materials	1
4.3	Domain theory – Hysteresis – soft and hard magnetic materials	1
4.4	Applications – Giant Magneto Resistance (*GMR*)	1
4.5	Electronic Polarization, Ionic Polarization	1
4.6	Orientational and space charge polarization	1
4.7	Frequency and Temperature dependence ofpolarization	1
4.8	Breakdown mechanisms	1
4.9	Applications of dielectrics in Capacitor and Transformer	1
5.0	**Advanced Materials and Nanotechnology**	
5.1	Metallic glasses – preparation, properties and applications	1
5.2	Shape memory alloys (SMA)	1
5.3	Characteristics, properties of NiTi alloy applications	1
5.4	Properties- Top-down process: Ball Milling method	1
5.5	Bottom-up process: Vapour Phase Deposition	1
5.6	Carbon Nano Tube (CNT): Properties	1
5.7	Preparation by electric arc method	1
5.8	CNT-Application	1
5.9	Single electron phenomena and Single electron transistor (SET)	1

Course Designer(s)

1. Dr. V. Vasudevan – vasudevanv@ksrct.ac.in
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60 CS 001	C Programming	Category	L	T	P	Credit
		ES	3	0	0	3

Objectives

- To learn most fundamental element of the C language and to examine the execution of branching, looping statements,
- To examine the concepts of arrays, its characteristics and types and strings.
- To understand the concept of functions, pointers and the techniques of putting them to use
- To apply the knowledge of structures and unions to solve basic problems in C language
- To enhance the knowledge in file handling functions for storage and retrieval of data

Pre-requisites

- NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Construct the fundamental building blocks of structured Programming in C	Apply
CO2	Implement the different operations on arrays and strings	Apply
CO3	Develop simple real world applications utilizing functions, recursion and pointers.	Apply
CO4	Demonstrate the concepts of structures, unions, user defined data types and preprocessor	Apply
CO5	Interpret the file concepts using proper standard library functions for a given application	Apply

Mapping with Programme Outcomes

Cos	Pos												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	2	2	-	2	3	3	2
CO2	3	3	3	-	3	-	-	-	2	2	-	2	3	3	2
CO3	3	3	3	-	3	-	-	-	2	2	-	2	3	3	2
CO4	3	3	3	-	3	-	-	-	2	2	-	2	3	3	2
CO5	3	3	3	-	3	-	-	-	2	2	-	2	3	3	2
1- low, 2- medium, 3- high															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	10	10	20
Apply	40	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

Common to All Branches

60 CS 001 – C Programming

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Basics of C, I/O, Branching and Loops* Structure of a C Program – Data types – Keywords – Variables – Type Qualifiers – Constants – Operators – expressions and precedence- Console I/O – Unformatted and Formatted Console I/O – Conditional Branching and Loops-Writing and evaluation of conditionals and consequent branching	[9]
Arrays and Strings* Arrays: One Dimensional Arrays – Two Dimensional Arrays – Matrix Manipulation – Character arrays – Strings: String Manipulation with and without String Handling Functions.	[7]
Functions and Pointers* Functions: Scope of a Function – Library Functions and User defined functions – Function Prototypes – Call by value and Call by reference – Function Categorization – Arguments to main function – Recursion and application – Passing Arrays to Functions – Storage class Specifiers. Introduction to Pointer Variables – The Pointer Operators – Pointer Expressions – Pointers and Arrays – Generating a Pointer to an Array – Indexing Pointers – Function and Pointers – Dynamic Memory Allocation.	[11]
Structures, Unions, Enumerations, Typedef and Preprocessors* Structures – Introduction to Structures and Initialization – Arrays of Structures – Arrays and Structures, Nested Structures – Passing Structures to Functions – Structure Pointers – Unions – Bit Fields – Enumerations – typedef –The preprocessor and commands.	[9]
File Handling* File: Streams –Reading and Writing Characters – Reading and Writing Strings – File System functions – File Manipulation-Sequential access – Random Access Files – Command Line arguments.	[9]
Total Hours:	**45**

Text Book(s):

1. Herbert Schildt, “The Complete Reference C”, 4th Edition, Tata McGraw Hill Edition, 2010.
2. Byron Gottfried, “Programming with C”, 3rd Edition, McGraw Hill Education, 2014.

Reference(s):

1. Balagurusamy. E, “Programming in ANSI C”, 7th Edition, Tata McGraw Hill Edition, New Delhi, 2016.
2. Brian W. Kernighan and Dennis M. Ritchie, “C Programming Language”, Prentice-Hall.
3. ReemaThareja, “Computer Fundamentals and Programming in C”, 2nd Edition, Oxford Higher Education, 2016.
4. King K N., “C Programming: A Modern Approach”, 2nd Edition, W.W.Norton, New York, 2008.

*SDG 4 – Quality Education

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Course Contents and Lecture Schedule

1	**Basics of C, I/O, Branching and Loops**	
1.1	Structure of a C Program, Keywords	1
1.2	Data types, Type Qualifiers	1
1.3	Variables and Constants	1
1.4	Operators-expressions and precedence	1
1.5	Console I/O- Unformatted and Formatted Console I/O	1
1.6	Conditional Branching	1
1.7	Iteration and loops	2
1.8	Writing and evaluation of conditionals and consequent branching	1
2	**Arrays and Strings**	
2.1	One Dimensional Array	1
2.2	Two-Dimensional Array and Matrix Manipulation	1
2.3	Character arrays and Strings Basics	1
2.4	String Manipulation without String Handling Functions	2
2.5	String Manipulation with String Handling Functions	2
3	**Functions and Pointers**	
3.1	Scope of a Function – Library Functions, User defined functions and Function Prototypes	1
3.2	Function Call by value and Function Call by reference, Function Categorization	2
3.3	Arguments to main function	1
3.4	Recursion and application	1
3.5	Passing Arrays to Functions	1
3.6	Storage class Specifiers	1
3.7	Introduction to Pointer Variables – The Pointer Operators – Pointer Expressions	1
3.8	Pointers and Arrays – Generating a Pointer to an Array – Indexing Pointers	1
3.9	Function and pointers	1
3.10	Dynamic Memory Allocation	1
4	**Structures, Unions, Enumerations, Typedef and Preprocessors**	
4.1	Introduction to Structures and Initialization	1
4.2	Arrays and Structures, Arrays of Structures	1
4.3	Structures within Structures, Passing Structures to Functions	2
4.4	Structure Pointers	1
4.5	Unions and Bit Fields.	1
4.6	Enumerations – typedef	1
4.7	Preprocessor commands	2
5	**File Handling**	
5.1	File Streams –Reading and Writing Characters – Reading and Writing Strings	2
5.2	File System functions and File Manipulation	2
5.3	Sequential access	2
5.4	Random Access Files	2
5.5	Command Line arguments and files	1
	Total Hours	**45**

Course Designers

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60 ME 005	Foundation of Mechanical Engineering	Category	L	T	P	Credit
		ES	3	0	0	3

Objectives

- To learn a process for analysis of static objects, concepts of force and motion of particles.
- To acquire knowledge on thermodynamics process, laws and entropy.
- To impart the concept of heat transfer mechanism through simple and composite geometries
- To learn the concept of refrigeration & Air-conditioning with its application.
- To identify the different sources of energy and to know the working principle of power plants.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply basic knowledge on static and dynamic systems.	Apply
CO2	Explain thermodynamic systems, properties and laws of thermodynamics.	Apply
CO3	Apply the principles of basic modes of heat transfer in solving heat transfer problems.	Apply
CO4	Identify the types of refrigeration and air-conditioning systems and explain its working principles.	Understand
CO5	Classify sources of energy and demonstrate method of power generation.	Understand

Mapping with Programme Outcomes

Cos	Pos												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	-	-	-	2	-	-	-	-	3	3	-
CO2	3	3	-	-	-	-	-	2	-	-	-	-	3	3	-
CO3	3	3	-	-	-	-	-	2	-	-	-	-	3	3	-
CO4	3	3	-	-	-	-	-	2	3	3	-	-	3	3	-
CO5	3	3	-	-	-	-	-	2	3	3	-	-	3	3	-
3 – Strong; 2 – Medium; 1 – Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	40	40	60
Apply	10	10	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R 2022

B.E – Electronics Engineering (VLSI Design and Technology)

Common to EE & ECE

60 ME 005 - Foundation of Mechanical Engineering

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	3	0	0	45	3	40	60	100

Basics of Statics and Dynamics of Particles Introduction - Units and Dimensions-Laws of Mechanics-Principle of Transmissibility - Lame'S Theorem, Parallelogram and Triangular Law of Forces. Displacement, Velocity, Acceleration and Their Relationship-Relative Motion.	[9]
Thermodynamics - Laws and Entropy Basic concepts - Thermodynamic systems - Laws of Thermodynamics: Zeroth Law of Thermodynamics, First Law of Thermodynamics - Second law of Thermodynamics - Cyclic Heat Engine, Heat Pump, Carnot Cycle. Entropy.	[9]
Heat Transfer Introduction - Modes of Heat Transfer: Conduction, Convection And Radiation - Laws of Conduction - Types of Convection- Laws of Radiation - Radiation Shields - Fourier Law of Heat Conduction In Simple And Composite Wall Geometrics, Types of Boundary and Initial Conditions - Fins: Types - Fin Efficiency.	[9]
Refrigeration and Air-Conditioning** Introduction - Terminology of Refrigeration and Air Conditioning Systems - Working Principle of Vapour Compression and Absorption System - Layout of Typical Domestic Refrigerator. Window, Split and Central Air Conditioners.	[9]
Sources of Energy* and Power Plants*** Introduction - Energy- Classification of Energy Sources - Conventional Energy Sources: Working Principle of Thermal, Gas, Diesel, Hydro-Electric and Nuclear Power Plants. Non - Conventional Energy Sources: Working Principle of Solar, Wind, Tidal and Geothermal Power Plants.	[9]
Total Hours:	**45**

Text Book(s):

1.	Pravin Kumar, ''Basic Mechanical Engineering", 2nd Edition, Pearson India Education Services Pvt. Ltd, Chennai, 2018.
2.	Rajasekaran, S., Sankarasubramanian, G., "Fundamentals of Engineering Mechanics", 3rd Edition Vikas Publishing House Pvt. Ltd., 2017.

Reference(s):

1.	YunusA.Cengel, ''Heat Transfer: A Practical Approach", 2nd Edition, Mcgraw-Hill, 2002.
2.	Arora.C.P. ''Refrigeration and Airconditioning", 3rd Edition, Tata McGraw Hill Education Pvt. Ltd., New Delhi, 2008.
3.	Arora, S. C., Domkundwar.S, ''A Course in Power Plant Engineering", Dhanpatrai& Co., New Delhi, 2014.
4.	Jayakumar, V. and Kumar, M, ''Engineering Mechanics", PHI Learning Private Ltd, New Delhi, 2012.

* SDG 7 - Affordable and Clean Energy

**SDG 9 - Industry Innovation and Infrastructure

***SDG 12 - Responsible Consumption and Production

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Basics of Statics and Dynamics of Particles**	
1.1	Introduction -Units and Dimensions	1
1.2	Laws of Mechanics-Principle of Transmissibility	1
1.3	Lame'S Theorem	1
1.4	Parallelogram Law of Forces	1
1.5	Triangular Law of Forces	1
1.6	Displacement, Velocity, Acceleration and Their Relationship	2
1.7	Relative Motion	2
2.0	**Thermodynamics - Laws and Entropy**	
2.1	Basic Concepts - Thermodynamic Systems	2
2.2	Laws of Thermodynamics: Zeroth Law of Thermodynamics, First Law of Thermodynamics	2
2.3	Laws of Thermodynamics: Second Law of Thermodynamics	1
2.4	Cyclic Heat Engine and Heat Pump	2
2.5	Carnot Cycle and Entropy	2
3.0	**Heat Transfer**	
3.1	Introduction to Heat Transfer	1
3.2	Modes of Heat Transfer: Conduction, Convection and Radiation	1
3.3	Laws of Conduction - Types of Convection- Laws of Radiation	1
3.4	Radiation Shields	1
3.5	Fourier Law of Heat Conduction In Simple Wall	1
3.6	Fourier Law of Heat Conduction In Composite Wall	1
3.7	Types of Boundary and Initial Conditions	1
3.8	Fins: Types and Efficiency	2
4.0	**Refrigeration and Air-Conditioning**	
4.1	Introduction to Refrigeration and Air-Conditioning and Its Terminology	2
4.2	Working Principle of Vapour Compression	1
4.3	Working Principle of Absorption System	1
4.4	Layout of Typical Domestic Refrigerator	2
4.5	Window and Split Air Conditioners.	2
4.6	Central Air Conditioners	1
5.0	**Sources of Energy and Power Plants**	
5.1	Introduction to Energy Resources and Classification	1
5.2	Working Principle of Thermal and Gas Power Plants	2
5.3	Working Principle of Diesel and Hydro-Electric Power Plants	2
5.4	Nuclear Power Plants	1
5.5	Working Principle of Solar and Wind Power Plants	2
5.6	Tidal and Geothermal Power Plants.	1

Course Designer(s)

1. Dr.A.Murugesan - murugesana@ksrct.ac.in
2. Mr.M.Gnanaseakran - gnanasekaran@ksrct.ac.in

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60 MY 001	Environmental Studies and Climate Change (Common to all)	Category	L	T	P	Credit
		MC	2	0	0	0

Objectives

- To understand the impact climate changes in ecosystem and biodiversity.
- To analyze the impacts of pollution, control and legislation.
- To explain the importance of sustainable development practices.
- To explore the significance of organic farming.
- To identify the Geo-spatial tools for resource management.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Interpret the impacts of pollution on climate change	Understand
CO2	Categorize the wastes and its management.	Analyze
CO3	Identify the different types of sustainable practices	Apply
CO4	Classify the organic farming techniques	Apply
CO5	Categorize the Geo-spatial tools for resource management	Analyze

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	-	-	3	-	-	-	-	2	2	-	-
CO2	3	2	-	-	-	3	3	2	-	-	-	2	2	3	-
CO3	3	2	-	-	-	3	3	2	-	-	-	2	2	3	-
CO4	3	2	-	-	-	2	3	-	-	-	-	2	-	-	-
CO5	3	2	-	-	3	-	2	-	-	-	-	2	2	3	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (30 Marks)		Quiz (20 marks)		Seminar presentation (50 marks)
	Case Study	Activity Report	Quiz 1	Quiz 2	
Remember	10	10	5	5	10
Understand	30	20	10	10	15
Apply	-	30	-	5	15
Analyse	20	-	5	-	10
Evaluate	-	-	-		-
Create	-	-	-		-
Total	60	60	20	20	50

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Common to all branches

60 MY 001 - Environmental Studies and Climate Change

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	2	0	0	30	0	100	-	100

Pollution and Its Impact on Climate Change* Pollution: Sources and Impacts of Air Pollution - Green House Effect- Global Warming- Climate Change - Ozone Layer Depletion - Acid Rain. Carbon Footprint - Climate Change on Various Sectors - Agriculture, Forestry and Ecosystem - Climate Change Mitigation and Adaptation. Action Plan on Climate Change. IPCC, UNFCCC, Kyoto Protocol, Montreal Protocol on Climatic Changes. *Activity*: Study of Carbon Emission Nearby Place or Industry.	[6]
Integrated Waste Management** Waste - Types and Classification. Principles of Waste Management (5R Approach) - Swachh Bharat Abhiyan - Commercial Waste, Plastic Waste, Domestic Waste, E-Waste and Biomedical Waste - Risk Management: Collection, Segregation, Treatment and Disposal Methods. Waste Water Treatment- ASP *Activity*: Analysis and Design Of Waste Management Systems, Prepare A Model / Project -Wealth From Waste	[6]
Sustainable Development Practices*** Sustainable Development Goals (Sdgs) - Green Computing- Carbon Trading - Green Building - Eco-Friendly Plastic - Alternate Energy: Hydrogen - Bio-Fuels - Solar Energy - Wind - Hydroelectric Power. Water Scarcity- Watershed Management, Ground Water Recharge and Rainwater Harvesting. *Activity*: Select A Topic and Analyze The Value of Sustainable Development.	[6]
Environment and Agriculture**** Organic Farming - Bio-Pesticides- Composting, Bio Composting, Vermi - Composting, Roof Gardening and Irrigation. Waste Land Reclamation. Climate Resilient Agriculture. Green Auditing *Activity*: Prepare A Green Auditing Report on Energy, Water Etc.	[6]
Geo-Science in Natural Resource Management Data Base Software in Environment Information, Digital Image Processing Applications in Forecasting. GPS, Remote Sensing and Geographical Information System (GIS), World Wide Web (Www), Environmental Information System (ENVIS). *Activity*: Prepare the Report Using IT Tool.	[6]
Total Hours:	**30**

Text Book(s):

1.	Anubha Kaushik , C P Kaushik. “Perspectives In Environmental Studies”, 6th Edition New Age International publishers; (1 January 2018).

Reference(s):

1.	Tyler Miller.G, “Environmental Science”, 14th Edition Cengage Publications, Delhi, 2013
2.	Gilbert M.Masters and Wendell P. Ela, “Environmental Engineering And Science”, 3rd Edition, PHI Learning Private Limited, 2015.
3.	Erach Bharucha. Textbook of Environmental Studies for Undergraduate Courses, Universities Press, 2000.

*SDG 13 - Climate Action
**SDG 4 - Clean Water and Sanitation
***SDG 6 - Affordable and Clean Energy
****SDG 3 - Good Health and Well-being

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Course Content and Lecture Schedule

S.No	Topic	No. of Hours
1	**Pollution and Its Impact on Climate Change**	
1.1	Pollution: Sources and Impacts of Air Pollution - Greenhouse Effect- Global Warming- Climate Change - Ozone Layer Depletion - Acid Rain	2
1.2	Climate Change on Various Sectors: Agriculture, Forestry and Ecosystem. - Climate Change Mitigation and Adaptation	2
1.3	Action Plan on Climate Change - IPCC, UNFCCC, Kyoto Protocol, Montreal Protocol On Climatic Changes	2
2	**Integrated Waste Management**	
2.1	Waste - Types and Classification. Principles of Waste Management (5R Approach) - Swachh Bharat Abhiyan	2
2.2	Commercial Waste, Plastic Waste, Domestic Waste, E-Waste and Biomedical Waste	2
2.3	Risk Management: Collection, Segregation, Treatment and Disposal Methods.	1
2.4	Waste Water Treatment- ASP	1
3	**Sustainable Development Practices**	
3.1	Sustainable Development Goals (Sdgs) **-** Green Computing- Carbon Trading - Green Building - Eco- Friendly Plastic	2
3.2	Alternate Energy: Hydrogen - Bio-Fuels - Solar Energy - Wind - Hydroelectric Power	2
3.3	Water Scarcity- Watershed Management, Ground Water Recharge and Rainwater Harvesting	2
4	**Environment and Agriculture**	
4.1	Organic Farming - Bio-Pesticides	2
4.2	Composting, Bio Composting, Vermi-Composting	2
4.3	Roof Gardening and Irrigation	1
4.4	Waste Land Reclamation. Climate Resilient Agriculture, Green Auditing	1
5	**Geo-Science In Natural Resource Management**	
5.1	Data Base Software in Environment Information, Digital Image Processing Applications in Forecasting	2
5.2	GPS, Remote Sensing and Geographical Information System (GIS)	2
5.3	World Wide Web (Www), Environmental Information System (ENVIS)	2
	Total	30

Course Designers

1. Dr.T.A.Sukantha - sukantha@ksrct.ac.in
2. Dr.S.Meenachi - meenachi@ksrct.ac.in
3. Mr.K.Tamilarasu - tamilarasu@ksrct.ac.in

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61 GE 001	தமிழர் மரபு (அனைத்து துறைகளும் பொதுவானது)	Category	L	T	P	Credit
		GE	1	0	0	1*

பாடத்தின் நோக்கங்கள்:

- தமிழ் மொழியின் இலக்கணச் செறிவைக் கற்றுணர்தல் ,வாழ்க்கைத் திறன்கள் மற்றும் நெறிமுறைகள் தெரிதல்.
- தமிழர் பண்பாட்டின் நுண்கலைகள் பற்றிய ஒரு மீள்பார்வை.
- தமிழர்களின் நாட்டுப்புறக்கலைகள் மற்றும் வீரவிளையாட்டுகள் குறித்து அறிதல்
- தமிழர்களின் திணைக் கோட்பாடுகள், சங்ககால வணிகம் மற்றும் சோழர்களின் வெற்றிகள் குறித்த தகவல்களை தெரிதல்.
- இந்திய சுதந்திரப் போராட்டத்தில் தமிழர்களின் பங்களிப்பை உணருதல்

முன்கூட்டிய துறை சார்அறிவு

தேவை இல்லை

பாடம் கற்றதின் விளைவுகள்

பாடத்தை வெற்றிகரமாக கற்றுமுடித்த பின்பு, மாணவர்களால் முடியும் விளைவுகள்

CO1	தமிழ் மொழியின் செந்தண்மை மற்றும் இலக்கியம் குறித்தும் . வாழ்க்கைத் திறன்கள் **மற்றும்** நெறிமுறைகள் குறித்தும் தெரிதல்	நினைவு கூர்தல் புரிதல் செயல் படுத்துதல்
CO2	தமிழர்களின் சிற்பக்கலை, ஓவியக்கலை மற்றும் இசைக்கருவிகள் குறித்த தெளிவு.	நினைவு கூர்தல் புரிதல்
CO3	தமிழர்களின் நாட்டுப்புறக்கலைகள் மற்றும் வீரவிளையாட்டுகள் குறித்த தெளிவு.	நினைவு கூர்தல் புரிதல்
CO4	தமிழர்களின் திணைக் கோட்பாடுகள், சங்ககால வணிகம் மற்றும் சோழர்களின் வெற்றிகள் குறித்த தகவல்கள்.	நினைவு கூர்தல் புரிதல்
CO5	இந்திய தேசிய இயக்கம், சுயமரியாதை இயக்கம் மற்றும் சித்த மருத்துவம் பற்றிய புரிதல்.	நினைவு கூர்தல் புரிதல்

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	2	-	3	2	-	-	1	-	-	-
CO2	-	-	-	-	-	1	1	1	-	-	-	3	-	-	-
CO3	-	-	-	-	-	2	-	3	3	2	-	2	-	-	-
CO4	2	-	-	-	-	1	1	2	1	2	-	1	-	-	-
CO5	-		-	-	-	-	-	3	2	2	-	2	-	-	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Test (Marks)	End Semester Examination (Marks)
Remember	40	40
Understand	40	40
Apply	20	20
Analysis	-	-
Evaluate	-	-
Create	-	-
Total	100	100

Note: Those who studied Tamil as language subject in +2 should write the exams (Model & End Semester Exams) in Tamil Language only. Those who did not study Tamil as language subject in +2 and other state students can write the exams in English Language. It is mandatory.

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Common to all Branches

61 GE 001 - Heritage of Tamils

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	1	0	0	15	1*	40	60	100

Language, Literature, Life Skills & Ethics* Language Families in India - Dravidian Languages – Tamil as a Classical Language - Classical Literature in Tamil – Secular Nature of Sangam Literature – Distributive Justice in Sangam Literature - Management Principles in Thirukural - Tamil Epics and Impact of Buddhism & Jainism in Tamil Land - Bakthi Literature Azhwars and Nayanmars - Forms of minor Poetry - Development of Modern literature in Tamil - Contribution of Bharathiyar and Bharathidhasan-Life, Responsibility, Self-exploration, Attitude, Self-confidence, Goals, Relationships, Leadership, Gender equality	[3]
Heritage - Rock Art Paintings to Modern Art – Sculpture* Hero stone to modern sculpture - Bronze icons - Tribes and their handicrafts - Art of temple car making -Massive Terracotta sculptures, Village deities, Thiruvalluvar Statue at Kanyakumari, Making of musical instruments - Mridhangam, Parai, Veenai, Yazh and Nadhaswaram - Role of Temples in Social and Economic Life of Tamils.	[3]
Folk and Martial Arts* Therukoothu, Karagattam, Villu Pattu, Kaniyan Koothu, Oyillattam, Leatherpuppetry, Silambattam, Valari, Tiger dance - Sports and Games of Tamils.	[3]
Thinai Concept of Tamils* Flora and Fauna of Tamils & Aham and Puram Concept from Tholkappiyam and Sangam Literature - Aram Concept of Tamils - Education and Literacy during Sangam Age - Ancient Cities and Ports of Sangam Age - Export and Import during Sangam Age - Overseas Conquest of Cholas.	[3]
Contribution of Tamils to Indian National Movement and Indian Culture* Contribution of Tamils to Indian Freedom Struggle - The Cultural Influence of Tamils over the other parts of India – Self-Respect Movement - Role of Siddha Medicine in Indigenous Systems of Medicine – Inscriptions & Manuscripts – Print History of Tamil Books.	[3]
Total Hours:	**15**

Text Book(s):

1.	முனைவர் கே. கே. பிள்ளை, தமிழக வரலாறு - மக்களும் பண்பாடும், தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம், 18th Ed ,2022.
2.	முனைவர் இல. சுந்தரம், கணினித்தமிழ்,விகடன் பிரசுரம், 2nd Ed 2021
3.	முனைவர் இரா.சிவானந்தம், மு.சேரன், கீழடி - வைகை நதிக்கரையில் சங்ககால நகர நாகரிகம், தொல்லியல் துறை வெளியீடு, 6th Ed ,2020.
4.	முனைவர் இரா.சிவானந்தம் , முனைவர் ஜெ.பாஸ்கர், பொருநை - ஆற்றங்கரை நாகரிகம், தொல்லியல் துறை வெளியீடு,1st Ed ,2022
5.	ஈரோடு கதிர் ,உயர்தல் உரிமை ,சிக்ஸ் ப்ளஸ் ஒன் ட்ரெயினிங் அகாடமி st1,Ed,2024
6.	Dr.K.K.Pillay, Social Life of Tamils, TNTB & ESC and RMRL – (In print).
7.	Dr.S.Singaravel, Social Life of the Tamils - The Classical Period, International Institute of Tamil Studies, 1st, 2001.
8.	Dr.S.V.Subaramanian, Dr.K.D. Thirunavukkarasu, Historical Heritage of the Tamils, International Institute of Tamil Studies, 2nd, 2010
9.	Dr.M.Valarmathi, The Contributions of the Tamils to Indian Culture, International Institute of Tamil Studies,
10.	Dr.R.Sivanantham, Keeladi - Sangam City Civilization on the banks of river Vaigai, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation,
11.	Dr.K.K.Pillay, Studies in the History of India with Special Reference to Tamil Nadu, K.K. Pillay(Published by the Author.
12.	Dr.R.Sivanantham, Dr.J.Baskar, Porunai Civilization, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.
13.	R.Balakrishnan, Journey of Civilization Indus to Vaigai, Roja Muthiah Research Library,3rd Ed, 2022

*SDG 4- Quality Education

*For Heritage of Tamils, additional 1 credit is offered and not accounted for CGPA

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61 GE 001 - *தமிழர் மரபு*

(அனைத்து துறைகளுக்கும் பொதுவானது)

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
I	1	0	0	15	1*	40	60	100

மொழி, இலக்கியம், வாழ்க்கைத் திறன்கள் மற்றும் நெறிமுறைகள்:* இந்திய மொழிக் குடும்பங்கள் - திராவிட மொழிகள் - தமிழ் ஒரு செம்மொழி - தமிழ் செவ்விலக்கியங்கள் - சங்க இலக்கியத்தின் சமயச் சார்பற்ற தன்மை - சங்க இலக்கியத்தில் பகிர்தல் அறம் - திருக்குறளில் மேலாண்மைக் கருத்துக்கள் - தமிழ் காப்பியங்கள் - தமிழகத்தில் சமண பௌத்த சமயங்களின் தாக்கம் - பக்தி இலக்கியம், ஆழ்வார்கள் மற்றும் நாயன்மார்கள் - சிற்றிலக்கியங்கள் - தமிழில் நவீன இலக்கியத்தின் வளர்ச்சி - தமிழ் இலக்கிய வளர்ச்சியில் பாரதியார் மற்றும் பாரதிதாசன் ஆகியோரின் பங்களிப்பு. வாழ்வியல், பொறுப்புணர்வு, சுய ஆய்வு, மனோபாவம், தன்னம்பிக்கை, இலக்குகள், உறவுகள், தலைமைப்பண்பு, பாலின சமநிலை.	[3]
***மரபு - பாறை ஓவியங்கள் முதல் நவீன ஓவியங்கள் வரை- சிற்பக் கலை.** * நடுகல் முதல் நவீன சிற்பங்கள் வரை - ஐம்பொன் சிலைகள் - பழங்குடியினர் மற்றும் அவர்கள் தயாரிக்கும் கைவினைப் பொருட்கள், பொம்மைகள் - தேர் செய்யும் கலை - சுடுமண் சிற்பங்கள் - நாட்டுப்புறத் தெய்வங்கள் - குமரிமுனையில் திருவள்ளுவர் சிலை - இசைக் கருவிகள் - மிருதங்கம், பறை, வீணை, யாழ், நாதஸ்வரம் - தமிழர்களின் சமூக பொருளாதார வாழ்வில் கோவில்களின் பங்கு.	[3]
***நாட்டுப்புறக் கலைகள் மற்றும் வீர விளையாட்டுகள்:** * தெருக்கூத்து, கரகாட்டம், வில்லுப்பாட்டு, கணியான் கூத்து, ஒயிலாட்டம், தோல்பாவைக் கூத்து சிலம்பாட்டம், வளரி, புலியாட்டம், தமிழர்களின் விளையாட்டுகள்.	[3]
***தமிழர்களின் திணைக் கோட்பாடுகள்:** * தமிழகத்தின் தாவரங்களும், விலங்குகளும் - தொல்காப்பியம் மற்றும் சங்க இலக்கியத்தில் அகம் மற்றும் புறக் கோட்பாடுகள் - தமிழர்கள் போற்றிய அறக்கோட்பாடு - சங்ககாலத்தில் தமிழகத்தில் எழுத்தறிவும், கல்வியும் - சங்ககால நகரங்களும் துறை முகங்களும் - சங்க காலத்தில் ஏற்றுமதி மற்றும் இறக்குமதி - கடல்கடந்த நாடுகளில் சோழர்களின் வெற்றி.	[3]
***இந்திய தேசிய இயக்கம் மற்றும் இந்திய பண்பாட்டிற்குத் தமிழர்களின் பங்களிப்பு:** * இந்திய விடுதலைப்போரில் தமிழர்களின் பங்கு - இந்தியாவின் பிறப்பகுதிகளில் தமிழ்ப் பண்பாட்டின் தாக்கம் - சுயமரியாதை இயக்கம் - இந்திய மருத்துவத்தில், சித்த மருத்துவத்தின் பங்கு - கல்வெட்டுகள், கையெழுத்துப்படிகள் - தமிழ் புத்தகங்களின் அச்சு வரலாறு	[3]
Total Hours:	**15**

Text Book(s):

1.	முனைவர் கே. கே. பிள்ளை, தமிழக வரலாறு - மக்களும் பண்பாடும், தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம், 18th Ed ,2022.
2.	முனைவர் இல. சுந்தரம், கணினித்தமிழ்,விகடன் பிரசுரம், 2nd Ed,2021
3.	முனைவர் இரா.சிவானந்தம், மு.சேரன், கீழடி - வைகை நதிக்கரையில் சங்ககால நகர நாகரிகம், தொல்லியல் துறை வெளியீடு, 6th Ed,2020.
4.	முனைவர் இரா.சிவானந்தம் , முனைவர் ஜெ.பாஸ்கர், பொருநை - ஆற்றங்கரை நாகரிகம், தொல்லியல் துறை வெளியீடு,1st Ed ,2022
5.	ஈரோடு கதிர் ,உயர்தல் உரிமை ,சிக்ஸ் ப்ளஸ் ஒன் ட்ரெயினிங் அகாடமி st1,Ed2024,
6.	Dr.K.K.Pillay, Social Life of Tamils, TNTB & ESC and RMRL – (In print).
7.	Dr.S.Singaravel, Social Life of the Tamils - The Classical Period, International Institute of Tamil Studies, 1st, 2001.
8.	Dr.S.V.Subaramanian, Dr.K.D. Thirunavukkarasu, Historical Heritage of the Tamils, International Institute of Tamil Studies, 2nd, 2010
9.	Dr.M.Valarmathi, The Contributions of the Tamils to Indian Culture, International Institute of Tamil Studies,
10.	Dr.R.Sivanantham, Keeladi - Sangam City Civilization on the banks of river Vaigai, Department o Archaeology & Tamil Nadu Text Book and Educational Services Corporation,
11.	Dr.K.K.Pillay, Studies in the History of India with Special Reference to Tamil Nadu, K.K. Pillay(Published by the Author.
12.	Dr.R.Sivanantham, Dr.J.Baskar, Porunai Civilization, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.
13.	R.Balakrishnan, Journey of Civilization Indus to Vaigai, Roja Muthiah Research Library,3rd Ed ,2022

*SDG 4 - Quality Education

* For Heritage of Tamils, additional 1 credit is offered and not accounted for CGPA.

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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Tiruchengode - 637 215

60 CS 0P1	C Programming Laboratory	Category	L	T	P	Credit
		ES	0	0	4	2

Objectives

- To enable the students to apply the concepts of C to solve simple problems
- To use selection and iterative statements in C programs
- To apply the knowledge of library functions in C programming
- To implement the concepts of arrays, functions, structures and pointers in C
- To implement the file handling operations through C

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Implement computational problems using selection and iterative statements	Apply
CO2	Demonstrate C program to manage collection of related data.	Apply
CO3	Design and implement different ways of passing arguments to functions, Recursion and implement pointers concepts.	Apply
CO4	Develop a C program to manage collection of different data using structures, Union, user-defined data types and preprocessor directives.	Apply
CO5	Demonstrate C program to store and retrieve data using file concepts.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	2	2	-	2	3	3	-
CO2	3	3	3	-	3	-	-	-	2	2	-	2	3	3	-
CO3	3	3	3	-	3	-	-	-	2	2	-	2	3	3	-
CO4	3	3	3	-	3	-	-	-	2	2	-	2	3	3	-
CO5	3	3	3	-	3	-	-	-	2	2	-	2	3	3	-
1- low, 2- medium, 3- high															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	12	-	-
Apply	50	13	100	100
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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K.S.Rangasamy College of Technology - Autonomous R2022								
Common to All Branches								
60 CS 0P1 - C Programming Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

List of Experiments:

1. Implementation of Simple Computational Problems Using Various Formulas*.
2. Implementation of Problems Involving Selection Statements*.
3. Implementation of Iterative Problems E.G., Sum of Series*.
4. Implementation of 1darray Manipulation*.
5. Implementation of 2D Array Manipulation*.
6. Implementation of String Operations*.
7. Implementationofsimplefunctionsanddifferentwaysofpassingargumentstofunctionsand Recursive Functions*.
8. Implementation of Pointers*.
9. Implementation of Structures and Union*.
10. Implementation of Bit Fields, Typedef and Enumeration*.
11. Implementation of Preprocessor Directives*.
12. Implementation of File Operations*.

* SDG:4 - Quality Education

Course Designer(s)

1. Dr.P.Kaladevi - kaladevi@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
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61 ME 0P1	Fabrication and Reverse Engineering Laboratory (Common to All branches)	Category	L	T	P	Credit
		ES	0	0	4	2

Objectives

- To provide hands-on training on Carpentry, Sheet metal, Fitting and Welding.
- To offer real time activity on plumbing connections and power tools in domestic applications.
- To provide hands-on training on CNC Wood Router and 3D Printing
- To provide hands-on training on household wiring and dismantling and assembling the home appliances.
- To offer real time activity on embedded programming using Arduino

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Make a wooden model using carpentry, Sheet metal Process.	Apply
CO2	Mate a model using filing and joining using MS Plate and repair & maintenances of water lines, power tools for home applications.	Apply
CO3	Cultivate the skills necessary for developing innovative and desirable products, including the ability to integrate user needs, market trends and technological advancement into the design process.	Apply
CO4	Trouble shoot the electrical and electronic circuits, electrical appliances and facilitate the house wiring.	Apply
CO5	Acquire practical knowledge on embedded programming using Arduino.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	3	-	-	2	2	-	3	-	-	3	-	3	3
CO2	3	2	3	-	-	2	2	-	3	-	-	3	-	3	3
CO3	3	2	3	-	-	2	2	-	3	-	-	3	-	3	3
CO4	3	-	3	-	-	2	2	-	3	-	-	3	-	3	3
CO5	3	-	3	-	-	2	2	-	3	-	-	3	-	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	25	12	50	50
Apply	25	13	50	50
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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K.S.Rangasamy College of Technology – Autonomous R2022								
(Common to All branches)								
61 ME 0P1 – Fabrication and Reverse Engineering Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
I	0	0	4	60	2	60	40	100

List of Experiments:

1. Making of Metal Model and Carpentry Process

a) Making of Tray using Sheet Metal Process

b) Making of T / Cross Joint using Carpentry Process.

2. Mating of Square Joint using the Filling Process

3. Fabrication of Welded model

4. Repair and Maintenance of Pipe Fitting for Home Applications

a) Assembly of GI pipes/PVC, Pipe Fitting and Cutting of Threads in GI pipes.

b) Fitting of Pipe with Clamps using Power Tools

5. Making of Model using CNC Wood Router

a) 2D profile cutting on plywood/MDF (6-12 mm) for press fit design

b) Machining of 3D geometry on soft material such as softwood

6. 3D Printing of scanned geometry using FDM or SLA Printer.

7. Dismantling and Assembling of

a) Iron Box

b) Mixer Grinder

c) Ceiling Fan

d) Table Fan

e) Water Heater

f) Induction Stove

8. Design and Execution of Residential house wiring with UPS.

a) 1 BHK

b) 2 BHK

9. Design and fabrication of domestic LED lamps

a) Schematic and PCB layout design of the given circuit and fabrication and testing of the same.

b) Soldering

10. Embedded programming using Arduino

Lab Manual	
1.	"Fabrication and Reverse Engineering Laboratory Manual", Department of Mechanical Engineering, KSRCT.

*SDG 9 – Industry Innovation and Infrastructure

Course Designer(s)

1. Mr.S Sakthivel - sakthivel_s@ksrct.ac.in
2. Dr.G.Vijayagowri - vijayagowri@ksrct.ac.in
3. Mr. K.Raguvaran - raguvaran@ksrct.ac.in

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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS

(For the candidates admitted in 2025-2026)

SECOND SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EN 002	Professional English II	2	40	60	100	45	100
2.	60 MA 003	Integrals, Partial Differential Equations and Laplace Transform	2	40	60	100	45	100
3.	60 CH 003	Chemistry For Electronic Engineering	2	40	60	100	45	100
4.	60 ME 002	Engineering Graphics	2	40	60	100	45	100
5.	60 EV 201	Electronic Devices	2	40	60	100	45	100
6.	60 GE 002	Tamils and Technology / தமிழரும்தொழில் நுட்பமும்	2	40	60	100	45	100
PRACTICAL								
7.	60 CP 0P2	Engineering Physics and Chemistry Laboratory	3	60	40	100	45	100
8.	60 EV 2P1	Electronic Devices Laboratory	3	60	40	100	45	100
9.	60 CG 0P1	Career Skill Development – I	1	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 for practical End Semester Examination.

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60 EN 002	Professional English II	Category	L	T	P	Credit
		HS	1	0	2	2

Objectives

- To help learners improve their vocabulary and enable them to use words appropriately in different academic and professional contexts.
- To help learners develop strategies that could be adopted while reading texts.
- To help learners acquire the ability to speak and write effectively in English in real life and career related situations.
- Improve listening, observational skills, and problem-solving capabilities
- Develop message generating and delivery skills

Pre-requisites

- Basic knowledge of reading and writing in English and should have completed Professional English I

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Compare and contrast products and ideas in technical texts.	Understand
CO2	Illustrate cause and effects in events, industrial processes through technical texts	Understand
CO3	Infer problems in order to arrive at feasible solutions and communicate them orally and in the written format.	Understand
CO4	Relate events and the processes of technical and industrial nature.	Remember
CO5	Demonstrate their opinions in a planned and logical manner, and draft effective résumés in context of job search.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO2	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO3	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3
CO4	-	-	-	-	-	-	-	2	3	3	2	3	3	3	3
CO5	-	-	-	-	-	-	-	2	3	3	2	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	50	80
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

Common to All Branches

60 EN 002 - Professional English II

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	1	0	2	45	2	40	60	100

Making Comparisons* **Listening:** Evaluative Listening: Advertisements, Product Descriptions, - Audio / Video; Filling A Graphic Organiser (Choosing A Product or Service by Comparison). **Speaking:** Marketing A Product, Persuasive Speech Techniques. **Reading:** Reading Advertisements, User Manuals and Brochures. **Writing:** Professional Emails, Email Etiquette - Compare and Contrast Essay. **Language Focus:** Mixed Tenses, Prepositional Phrases, Same Words Used In Different Contexts And Discourse Markers	[9]
Expressing Causal Relations in Speaking and Writing* **Listening:** Listening to Longer Technical Talks and Completing - Gap Filling Exercises. Listening Technical Information from Podcasts - Listening to Process/Event Descriptions to Identify Cause & Effects. **Speaking:** Describing and Discussing the Reasons of Accidents or Disasters Based on News Reports. **Reading:** Longer Technical Texts - Cause and Effect Essays, and Letters / Emails of Complaint, **Writing:** Writing Responses to Complaints. **Language Focus:** Active Passive Voice Transformations, Infinitive and Gerunds - Word Formation (Noun-Verb-Adj-Adv), Adverbs.	[9]
Problem Solving* **Listening:** Listening to / Watching Movie Scenes/ Documentaries Depicting a Technical Problem and Suggesting Solutions. **Speaking:** Group Discussion (Based on Case Studies), - Techniques and Strategies. **Reading:** Case Studies, Excerpts from Literary Texts, News Reports Etc. **Writing:** Letter to the Editor, Checklists, Problem Solution Essay / Argumentative Essay. **Language Focus:** Error Correction; If Conditional Sentences - Compound Words, Sentence Completion.	[9]
Reporting of Events and Research* **Listening:** Listening Comprehension Based on New Report and Documentaries - **Speaking:** Interviewing, Presenting Oral Reports, Mini Presentations on Select Topics. **Reading:** Newspaper Articles. **Writing:** Recommendations, Transcoding, Accident Report, Precis Writing and Summarising and Plagiarism. **Language Focus:** Reported Speech - Modals - Conjunctions- Use of Prepositions	[9]
The Ability to Put Ideas or Information Coherently* **Listening:** Listening to TED Talks, Presentations, Formal Job Interviews, (Analysis of The Interview Performance). **Speaking:** Participating in Role Plays, Virtual Interviews, Making Presentations with Visual Aids. **Reading:** Excerpts of Interview with Professionals **Writing:** Job / Internship Application - Cover Letter & Resume. **Language Focus:** Numerical Adjectives, Question Types: Wh/ Yes or No/ and Tags; Relative Clauses - Idioms.	[9]
Total Hours:	45

Text Book(s):	
1.	‘‘English for Engineers & Technologists, “Orient Blackswan Private Ltd. Department of English, Anna University, 2020.
2.	Norman Lewis, ‘‘Word Power Made Easy - The Complete Handbook for Building a Superior Vocabulary Book‘‘, Penguin Random House India, 2020.
Reference(s):	
1.	Raman. Meenakshi, Sharma. Sangeeta, “Professional English”, Oxford university press. New Delhi. 2019.
2.	Arthur Brookes and Peter Grundy, “Beginning to Write: Writing Activities for Elementary and Intermediate Learners”, Cambridge University Press, New York, 2003
3.	Prof. R.C. Sharma & Krishna Mohan, ‘‘Business Correspondence and Report Writing”, Tata McGraw Hill & Co. Ltd., New Delhi, 2001
4.	V.N. Arora and Laxmi Chandra, ‘‘Improve Your Writing”, Oxford University Press, New Delhi, 2001

* SDG 4 - Quality Education

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Making Comparisons**	
1.1	Evaluative Listening	1
1.2	Product Descriptions and Filling A Graphic Organiser	1
1.3	Marketing A Product by Using Persuasive Techniques	2
1.4	Reading Advertisements, User Manuals and Brochures	1
1.5	Writing Professional Emails	1
1.6	Compare and Contrast Essay	1
1.7	Mixed Tenses and Prepositional Phrases	1
1.8	Same Words Used in Different Contexts	1
2	**Expressing Causal Relations in Speaking and Writing**	
2.1	Listening to Longer Technical Talks	1
2.2	Listening to Process/Event Descriptions	1
2.3	Describing and Discussing the Reasons of Accidents or Disasters	1
2.4	Reading Longer Technical Texts- Cause and Effect Essays	1
2.5	Writing Responses to Complaints	1
2.6	Active Passive Voice Transformations	2
2.7	Infinitive and Gerunds	1
2.8	Word Formation (Noun-Verb-Adj-Adv), Adverbs.	1
3	**Problem Solving**	
3.1	Listening to Documentaries and Suggesting Solutions	1
3.2	Group Discussion (Based on Case Studies)	2
3.3	Reading Case Studies, Excerpts from Literary Texts and News Reports	1
3.4	Letter to The Editor	1
3.5	Checklists	1
3.6	Problem Solution and Argumentative Essays	1
3.7	Error Correction and Sentence Completion, If Conditional Sentences	2
4	**Reporting of Events and Research**	
4.1	Listening Comprehension	1
4.2	Interviewing and Presenting Oral Reports	1
4.3	Mini Presentations on Select Topics	1
4.4	Reading Newspaper Articles	
4.5	Recommendations	1
4.6	Transcoding	1
4.7	Precis Writing, Summarising and Plagiarism	1
4.8	Reported Speech, Modals	1
4.9	Conjunctions	1
5	**The Ability to put Ideas or Information Coherently**	
5.1	Listening to Formal Job Interviews	1
5.2	Role Plays	2
5.3	Virtual Interviews	1
5.4	Reading Company Profiles	1
5.5	Writing Statement of Purpose (Sops)	1
5.6	Writing Résumé	1
5.7	Numerical Adjectives and Relative Clauses - Idioms	1
5.8	Question Types: Wh/ Yes or No/ And Tags	1

Course Designer(s)

1. Dr.A.Palaniappan -palaniappan@ksrct.ac.in

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60 MA 003	Integrals, Partial Differential Equations and Laplace Transform	Category	L	T	P	Credit
		BS	3	1	0	4

Objectives

- To acquire the knowledge about multiple integrals
- To familiarize the basic concepts of vector calculus
- To get exposed to the fundamentals of analytic functions
- To solve various types of partial differential equations.
- To familiarize the concepts of Laplace transform

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Interpret the basic concepts of double and triple integrals.	Apply
CO2	Interpret the basic concepts of vector calculus.	Apply
CO3	Construct the Analytic functions and evaluate the complex integrals.	Apply
CO4	Compute the solutions of partial differential equations using different methods.	Apply
CO5	Apply Laplace transform techniques for solving differential equations.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO5	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	20
Apply	40	40	70
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

Common to Mech, ECE, EE, EEE, CSE, MCT, CIVIL, IT, TXT, BT, FT

60 MA 003 - Integrals, Partial Differential Equations and Laplace Transform

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	1	0	60	4	40	60	100

Multiple Integrals Double Integration - Cartesian and Polar Co-Ordinates - Change of Order of Integration - Area as Double Integral - Triple Integration in Cartesian Co-Ordinates - Change of Variables - Cartesian to Polar Co-Ordinates and Cartesian to Cylindrical Co-Ordinates. **Hands - on:** Evaluating double integrals, triple integrals, area as double integrals and volume as triple integrals	[9]
Vector Calculus* Introduction - Gradient of a Scalar Point Function -Directional Derivative - Angle of Intersection of Two Surfaces - Divergence and Curl (Excluding Vector Identities) - Solenoidal and Irrotational Vectors - Application: Green's Theorem In The Plane - Gauss Divergence Theorem -Stokes' Theorem (Statement Only) **Hands - On:** Evaluating Gradient, Divergence and Curl.	[9]
Analytic Functions and Integrals Analytic Function - Necessary and Sufficient Conditions (Statement Only)-Properties - Harmonic Function - Construction of An Analytic Function - Cauchy's Integral Theorem (Statement Only) - Cauchy's Integral Formula - Classification of Singularities - Application: Cauchy's Residue Theorem. **Hands - on**: Plotting and visualizing functions of single variable, two and three variables.	[9]
Partial Differential Equations* Formation of Partial Differential Equations by Eliminating Arbitrary Constants and Arbitrary Functions - Non- Linear Partial Differential Equations of First Order - Lagrange's Linear Equations - Application: Homogeneous Linear Partial Differential Equations with Constant Coefficients. **Hands - on**: Calculate homogeneous linear partial differential equations.	[9]
Laplace Transform Conditions for Existence - Transforms of Elementary Functions - Basic Properties - Derivatives and Integrals of Transforms - Initial and Final Value Theorem - Transform of Periodic Functions. Inverse Laplace Transform - Convolution Theorem (Excluding Proof) - Application: Solution of Second Order Ordinary Differential Equations with Constant Co-Efficients. **Hands - on:** Evaluating laplace, Inverse laplace transforms and solve differential equations.	[9]
Total Hours: 45 + 5(Hands on) + 10(Tutorial):	**60**

Text Book(s):

1. Grewal B.S, "Higher Engineering Mathematics", 44th Edition, Khanna Publishers, Delhi, 2017.
2. Kreyszig Erwin, "Advanced Engineering Mathematics", 10th Edition, John Wiley and Sons (Asia) Limited,New Delhi, 2016.

Reference(s):

1. Dass H.K, "Higher Engineering Mathematics", 3rd (Revised) Edition, S.Chand& Company Ltd, New Delhi, 2014.
2. Veerarajan T, "Engineering Mathematics", for Semesters I & II, 1st Edition, Tata McGraw Hill Publishing Co., New Delhi, 2019.
3. Kandasamy P, Thilagavathy K and Gunavathy K, "Engineering Mathematics - I", S.Chand& Company Ltd, New Delhi, 2017.
4. Bali N P and Manish Goyal, A text book of Engineering Mathematics",10th Edition, Laxmi Publications(P) Ltd, 2016.

*SDG4 : Quality Education

Passed in BoS Meeting held on 13/06/2025
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Department of Electronics Engineering
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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Multiple Integrals**	
1.1	Double integration	1
1.2	Cartesian and polar coordinates	1
1.3	Change of order of integration	1
1.4	Area as double integral	1
1.5	Triple integration in Cartesian coordinates	1
1.6	Change of variables	2
1.7	Cartesian to polar coordinates	1
1.8	Cartesian to Cylindrical coordinates	1
1.9	Tutorial	2
1.10	Hands on	1
2	**Vector Calculus**	
2.1	Introduction: Gradient of a scalar point function	1
2.2	Directional derivative	1
2.3	Angle of intersection of two surfaces	1
2.4	Divergence and curl (excluding vector identities)	1
2.5	Solenoidal and irrotational vectors	1
2.6	Application: Green's theorem in the plane	1
2.7	Gauss divergence theorem	2
2.8	Stokes' theorem (statement only)	1
2.9	Tutorial	2
2.10	Hands on	1
3	**Analytic Functions and Integrals**	
3.1	Analytic function	1
3.2	Necessary and Sufficient conditions (statement only)	1
3.3	Properties	1
3.4	Harmonic function	1
3.5	Construction of an analytic function	1
3.6	Cauchy's Integral theorem (statement only), Cauchy's integral formula	2
3.7	Classification of singularities	1
3.8	Applications : Cauchy's residue theorem.	1
3.9	Tutorial	2
3.10	Hands on	1
4	**Partial Differential Equations**	
4.1	Formation of partial differential equations by eliminating arbitrary constants	1
4.2	Formation of partial differential equations by eliminating arbitrary functions	2
4.3	Non- linear partial differential equations of first order	3
4.4	Lagrange's linear equations	1
4.5	Application: Homogeneous Linear partial differential equations with constant coefficients.	2
4.6	Tutorial	2
4.7	Hands on	1
5	**Laplace Transform**	
5.1	Conditions for existence	1
5.2	Transforms of elementary functions	1
5.3	Basic properties	1
5.5	Derivatives and integrals of transforms, Initial and final value theorem	1
5.6	Transform of periodic functions	1
5.7	Inverse Laplace transform	1
5.8	Convolution theorem (excluding proof)	1
5.9	Application: Solution of second order ordinary differential equation with constant co-efficient.	2
5.10	Tutorial	2
5.11	Hands on	1

Course Designer(s)

1. Dr. C. Chandran - cchandran@ksrct.ac.in
2. Dr. K. Prabakaran - prabakaran@ksrct.ac.in

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60 CH 003	Chemistry for Electronic Engineering	Category	L	T	P	Credit
		BS	3	0	0	3

Objectives

- To help the learners to analyse the hardness of water and its removal
- To study the concepts of electrochemistry and its applications
- To study the types of batteries and fuel cells.
- To explain the characteristics and application of chemical sensors
- To study the working principles of smart materials and its applications

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Identify the types of hardness of water and its removal.	Apply
CO2	Interpret the applications of electro chemistry.	Understand
CO3	Illustrate the significance of the types of batteries and fuel cells.	Understand
CO4	Categorize the types of sensors for various applications.	Apply
CO5	Identify the properties, principles, and applications of various smart materials in modern technologies.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	-	-	-	-	-	-	-	-	3	-	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-	2	2	-
CO5	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom''s Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	20
Understand	30	40	60
Apply	10	-	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

B.E – EEE, ECE & EE (VLSIDT)

60 CH 003 - Chemistry for Electronic Engineering

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Water Technology* Introduction – Commercial and Industrial uses of Water - Hardness - Types – Estimation of Hardness by EDTA Method- Internal Conditioning (Colloidal, Phosphate, Calgon and Carbonate Conditioning Methods) – External Conditioning (Zeolite Process, Demineralization Process) - Desalination Methods (Reverse Osmosis and Electro Dialysis) - Flash Evaporation.	[9]
Electrochemistry ** Electrode Potential - Nernst Equation - Derivation and Problems - Reversible and Irreversible Cells - Types of Electrodes and its Applications - Reference Electrodes - pH, Conductometric and Potentiometric Titrations - Principles of Electro Plating and Electro Less Plating- Fabrication Process of Printed Circuit Board.	[9]
Energy Storage Devices ** ,*** & **** Batteries - Types of Batteries. Fabrication and Working of Alkaline Battery - Lead-Acid Battery-Ni-Cd-Lithium Ion Batteries – Fuel Cells: Hydrogen-Oxygen fuel cell - microbial fuel cell (MFC). Organic Solar Cells-working principle and applications organic transistors-construction-working principle and applications in electronic Industries.	[9]
Chemical Sensors*** Sensors - Chemical Sensors - Characteristics - Elements and Characterization - Potentiometric Sensors - Amperometric Sensors - Sensors Based on Electrochemical Methods - Electrochemical Biosensors – Optical Biosensors: Enzyme Sensors - Bio Affinity Sensors - DNA Sensors. Chemical Sensors as Detectors and Indicators: Indicators for Titration Processes - Separation Methods - Nano Technology in Chemical Sensors.	[9]
Electronic Materials *** Liquid Crystal Polymers - Organic Light Emitting Diode - Polythiopene - Working and Applications - Conductive Polymers and Semi Conducting Polymers - Principle and Applications - Organic Dielectric Material [Polystyrene, Pmma] - Smart Screen Materials: Inorganic Rare Earth Metals [Yttrium, Lanthanum, Cerium] - Conductive Components: Indium Tin Oxide [Properties and Applications] - Touch Screen [Resistive and Capacitive] - Magnetic Storage [Iron Oxide, Cobalt Alloy] – Optical Storage [Photo Chromic Materials] - Solid Storage.	[9]
Total Hours:	**45**

Text Book(s):

1. Palanna O.G. "Engineering Chemistry" Tata McGraw-Hill Pub.Co.Ltd, New Delhi, 2017.
2. Jain. P.C. and Monica Jain, "Engineering Chemistry", 14th Edition, Dhanpatrai publishing co. New Delhi, 2015.

Reference(s):

1. Pletcher D and Walsh F C, "Industrial Electrochemistry", 2nd Edition, Chapman and Hall, New York, 1990
2. Roussak O.V. and H.D. Gesser, "Applied Chemistry-A Text Book for Engineers and Technologists", 2nd Edition, Springer Science Business Media, New York, 2013.
3. Shikha Agarwal, "Engineering Chemistry-Fundamentals and Applications", 2nd Edition, Cambridge University Press, Delhi, 2019.
4. Hagen Klauk, "Organic Electronics: Materials, Manufacturing and Applications", Wiley-VCH, 2006.

* SDG 6 - Improve Clean Water and Sanitation
**SDG 7 - Affordable and clean energy
***SDG 9 - Industry, innovation and infrastructure
****SDG - 12 Responsible consumption and production

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Water Technology**	
1.1	Introduction – Commercial and Industrial uses of water	**1**
1.2	Hardness - types	**1**
1.3	Estimation of Hardness of water by EDTA method	**1**
1.4	Internal conditioning (Colloidal, Phosphate, Calgon and Carbonate)	**1**
1.5	External conditioning (Zeolite process)	**1**
1.6	Demineralization process	**1**
1.7	Desalination methods - Reverse Osmosis	**1**
1.8	Electro dialysis	**1**
1.9	Flash Evaporation	**1**
2.0	**Electrochemistry**	
2.1	Electrode potential - Nernst Equation - derivation and problems	**2**
2.2	Reversible and irreversible cells	**1**
2.3	Types of Electrodes and its applications	**1**
2.4	Reference electrodes - pH	**1**
2.5	Conductometric and Potentiometric titrations	**1**
2.6	Principles of electro plating and electro less plating-	**2**
2.7	Fabrication process of Printed Circuit Board.	**1**
3.0	**Energy Storage Devices**	
3.1	Batteries - Types of Batteries.	**2**
3.2	Fabrication and Working of Alkaline Battery	**1**
3.3	Lead-Acid Battery	**1**
3.4	Ni-Cd-Lithium Ion Batteries	**1**
3.5	Fuel Cells: Hydrogen-Oxygen fuel cell	**1**
3.6	Microbial fuel cell (MFC).	**1**
3.7	Organic Solar Cells-working principle and applications organictransistors	**1**
3.8	Consruction-working principle and applications in electronic Industries.	**1**
4.0	**Chemical Sensors**	
4.1	Sensors – Chemical Sensors - Characteristics	**1**
4.2	Elements and Characterization	**1**
4.3	Potentiometric Sensors, Amperometric Sensors	**1**
4.4	Sensors Based on Electrochemical Methods	**1**
4.5	Electrochemical Biosensors	**1**
4.6	Optical Biosensors: Enzyme Sensors – Bio affinity Sensors	**1**
4.7	DNA Sensors. Chemical Sensors as Detectors and Indicators	**1**
4.8	Indicators for Titration Processes	**1**
4.9	Separation Methods. Nano technology in chemical sensors.	**1**
5.0	**Electronic Materials**	
5.1	Liquid crystal polymers - Organic Light Emitting Diode (OLED) - [polythiopene] - working and applications	**2**
5.2	Conductive polymers and Semi conducting polymers: principle and applications	**2**
5.3	Organic: Organic dielectric material [Polystyrene, PMMA].	**1**
5.4	Smart screen materials: Inorganic Rare earth metals [yttrium, lanthanum, cerium]	**1**
5.5	Conductive components: Indium tin oxide [properties and applications] - touch screen [resistive and capacitive]	**1**
5.6	Magnetic storage [Iron oxide, cobalt alloy]	**1**
5.7	Optical storage [photo chromic materials] - solid storage.	**1**

Course Designer(s)

1. Dr.T.A.Sukantha - sugantha@ksrct.ac.in
2. Dr.B.Srividhya - srividhyab@ksrct.ac.in
3. Dr.S.Meenachi - meenachi@ksrct.ac.in
4. Ms.D.Kirthiga - kiruthiga@ksrct.ac.in

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60 ME 002	Engineering Graphics	Category	L	T	P	Credit
		ES	2	0	4	4

Objectives

- To acquire various concepts of dimensioning, conventions and standards.
- To impart the graphic skills for converting pictorial views of solids in to orthographic views.
- To learn the concept in projection of solids, section of solids and development of different types of surfaces.
- To learn the concept of isometric projection.
- To learn the geometry and topology of engineered components

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Demonstrate the Impact of computer technologies on graphical communication	Apply
CO2	Convert the pictorial views in to orthographic views using drafting software	Apply
CO3	Draw the projection of simple solids, true shape of sections and development of surfaces	Apply
CO4	Construct the isometric projections of objects using drafting software.	Apply
CO5	Interpret a design project illustrating engineering graphical skills.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	3	-	3	-	-	-	-	-	-	-	2	3	-
CO2	3	3	3	-	3	-	-	-	-	-	-	-	2	3	-
CO3	3	3	3	-	3	-	-	3	-	-	-	-	2	3	-
CO4	3	3	3	-	3	-	-	3	-	-	-	-	2	3	-
CO5	3	3	3	-	3	-	-		-	-	-	-	2	3	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	20	20	30
Apply	30	30	50
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 ME 002 - Engineering Graphics

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	2	0	4	90	4	40	60	100

Introduction to Computer Aided Drafting (CAD) software* Theory of CAD software - Menu System, Tool bars (Standard, Object Properties, Draw, Modify and Dimension) - Drawing Area (Background, Crosshairs, Coordinate System) - Dialog boxes and windows - Shortcut menus (Button Bars) - The Command Line and Status Bar - Different Methods of Zoom - Select and Erase Objects.	[6+12]
Orthographic Projection* Theory of projection - Terminology and Methods of Projection - First Angle and Third Angle Projection - Conversion of Pictorial Views into Orthographic Views	[6+12]
Projection of Solids and Sections of Solids* Projections of Simple Solids: Prism, Pyramid, Cylinder and Cone (Axis Parallel to One Plane and Perpendicular to Other, Axis Inclined to One Plane and Parallel to Other). Sections of Simple Solids: Prism, Pyramid, Cylinder and Cone In Simple Positions (Cutting Plane is Inclined to One of the Principal Planes and Perpendicular To The Other) - True Shape of Sections **Development of Surfaces*** Principle of development-Methods of development: Parallel line development-Cube, Prism and Cylinder. Radial Line Development - Pyramid and Cone	[6+12]
Isometric Projection* Principles of Isometric Projection - Isometric Scale, Isometric Views, Conventions - Isometric Views of Lines, Planes, Simple and Compound Solids - Conversion of Orthographic Views in to Isometric View	[6+12]
Application of Engineering Graphics* Geometry and Topology of Engineered Components: Creation of Engineering Models and their Presentation in Standard 2D Blueprint Form, 3D Wire-Frame and Shaded Solids - Geometric Dimensioning and Tolerance - Use of Solid Modeling Software for Creating Associative Models - Floor Plans: Windows, Doors, and Fixtures such as Water Closet (WC), Bath Sink, Shower, Etc. - Applying Colour Coding According to Building Drawing Practice - Drawing Sectional Elevation Showing Foundation to Ceiling - Introduction To Building Information Modelling (BIM).	[6+12]
Total Hours: (Lecture - 30; Practical - 60)	**90**

Text Book(s):

1.	Bhatt N.D., “Engineering Drawing”, 53rd Edition, Charotar Publishing House Pvt. Ltd., Gujarat, 2019.
2.	Venugopal K., “Engineering Graphics”, New Age International (P) Limited, 2014.

Reference(s):

1.	Shah M.B., Rana B.C., and Jadon V.K., “Engineering Drawing”, Pearson Education, 2011.
2.	Natarajan K.V., “A Text Book of Engineering Graphics”, Dhanalakshmi Publishers, Chennai, 2014.
3.	Agrawal B. & Agrawal C. M., “Engineering Graphics”, TMH Publication, 2012.
4.	Narayana, K.L. & Kannaiah P, “Text book on Engineering Drawing”, Scitech Publishers, 2008.

*SDG 9 - Industry Innovation and Infrastructure

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Tiruchengode - 637 215

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1	**Introduction to Computer Aided Drafting (CAD) software**	
1.1	Theory of CAD Software	1
1.2	Menu System, Tool Bars (Standard, Object Properties, Draw, Modify and Dimension)	1
1.3	Drawing Area (Background, Crosshairs, Coordinate System)	1
1.4	Dialog Boxes And Windows - Shortcut Menus	1
1.5	The Command Line And Status Bar	1
1.6	Different Methods of Zoom - Select and Erase Objects.	2
2	**Orthographic Projection**	
2.1	Introduction to Orthographic Projections	2
2.2	Planes of Projection,	2
2.3	Projection of Points	1
2.4	Projection of Lines Inclined to Both Planes.	2
2.5	Projection of Planes	2
2.6	Projection of Planes Inclined to Both Planes	1
2.7	Conversions of Pictorial Views to Orthographic Views.	3
2.8	Practice Class for Pictorial Views to Orthographic Views.	2
2.9	Practice Class for Pictorial Views to Orthographic Views.	1
3	**Projection of Solids**	
3.1	Projections of Simple Solids: Prism	2
3.2	Projections of Simple Solids: Cylinder	3
3.3	Projections of Simple Solids: Pyramid	2
3.4	Projections of Simple Solids: Cone	2
3.5	Practice Class for Projection of Solids	2
3.6	Axis of Solid Inclined to Both HP and VP	5
3,7	Section of Solids for Prism,	2
3,8	Section of Solids for Cylinder,	2
3,9	Section of Solids for Pyramid,	2
3,10	Section of Solids for Cone	2
3,11	Auxiliary Views - Draw The Sectional Orthographic Views of Geometrical Solids.	3
3.12	Draw the Sectional Orthographic Views of Objects From Industry.	3
3,13	Development of Surfaces of Right Solids Prism,	2
3.14	Development of Surfaces of Right Solids Pyramid	2
3.15	Development of Surfaces of Right Solids Cylinder And Cone	2
4	**Isometric Projection and Introduction to AutoCAD**	
4.1	Principles of Isometric Projection	1
4.2	Isometric Scale	2
4.3	Isometric Projections of Simple Solids: Prism,	2
4.4	Isometric Projections of Simple Solids: Pyramid,	2
4.5	Isometric Projections of Simple Solids: Cylinder	1
4.6	Isometric Projections of Simple Solids: Cone	2
4.7	Isometric Projections of Frustum	2
4.8	Isometric Projections of Truncated Solids	2
4.9	Combination of Two Solid Objects In Simple Vertical Positions.	3
5	**Application of Engineering Graphics**	
5.1	Geometry and Topology of Engineered Components:	2
5.2	Creation of Engineering Models and Their Presentation In Standard 2D Blueprint Form,	3
5.3	3D Wire-Frame and Shaded Solids - Geometric Dimensioning and Tolerance - Use of Solid Modelling Software for Creating Associative Models	3
5.4	Floor Plans: Windows, Doors, and Fixtures Such as Water Closet (WC), Bath Sink, Shower, Etc.	3
5.5	Applying Colour Coding According to Building Drawing Practice	2
5.6	Drawing Sectional Elevation Showing Foundation to Ceiling	2
5.7	Introduction to Building Information Modelling (BIM).	2

Course Designer(s)

1. Dr.K. Mohan-mohank@ksrct.ac.in

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Chairman - Board of Studies
Department of Electronics Engineering
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60 EV 201	Electronic Devices (Common to ECE and EE)	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To understand the physics of junction diodes and to learn to implement them in various applications
- To learn different configurations of BJT and FET and applications of MOSFET
- To identify the use of various transducers and sensors.
- To study the construction and operation of various opto devices
- To familiarize the operation of power devices and convertors

Pre-requisites

- Physics for Electrical Engineering

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Construct circuits with diodes for various applications	Apply
CO2	Discuss the operation of transistors and their configurations	Understand
CO3	Identify the type of transducers and sensors used for various application	Understand
CO4	Explain the operation of various opto devices	Understand
CO5	Discuss the operation of power electronics devices and convertors and their applications	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	2	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	2	3
CO3	3	2	-	-	-	-	-	3	3	3	-	-	3	2	3
CO4	3	2	-	-	-	-	-	3	3	3	-	-	3	2	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	50
Understand	40	50	40
Apply	10	-	10
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

B.E - Electronics Engineering (VLSI Design and Technology) Common to ECE and EE

60 EV 201 - Electronic Devices

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	3	0	0	45	3	40	60	100

Diodes* PN junction diode- Current Voltage Characteristics and Analysis, Diode Logic Gates, Modelling the Diode Forward Characteristics- Graphical analysis, Small Signal Model, Zener Diode, Varactor Diode and Diode Applications. **Hands - on:** 1. Simulation of VI characteristics of PN junction diode	[9]
Transistors* Construction and Operation of a Transistor, Input and Output Characteristics of a Transistor in CE configuration, operation of CB and CC configurations, Construction and Characteristics of n channel JFET, Basic MOSFET operation, Characteristics of Depletion type MOSFET and Enhancement Type MOSFET and MOSFET applications.** **Hands - on:** 1. Simulation of input- output characteristics of BJT 2. Simulation of I-V characteristics of MOSFET	[9]
Transducers and Sensors* Classification of Transducers, Transducers Actuating Mechanisms, Resistance Transducers, Variable Inductance Transducers, Capacitive Transducers, Piezoelectric Transducers, Hall Effect Transducers, Noise introduced by Transducers and Their Reduction. Smart Sensors, Fiber Optic Sensors, MEMS, Ultrasonic Sensors and Their Typical Applications	[9]
Opto Devices* Introduction, Photo emitters, LASER, LED, Photoconductive Cell, Opto coupler, Solid state relays (light operated relay) and optical fibre***.	[9]
Power devices and Convertors* Construction and Operation of Switching Devices - SCR, MOSFET and IGBT** - Static Characteristics of SCR - Switching Mode Regulators: Buck Regulator, Boost Regulator, Buck-Boost Regulators, Chopper***	[9]
Total Hours:	45

Text Book(s):

1.	Anil K. Maini, Varsha Agrawal, ‘‘Electronics Devices and Circuits’‘, 2nd Edition, Wiley India Pvt.Ltd, 2019.
2.	Patranabis. D, “Sensors and Transducers”, Prentice Hall of India, 1999
3.	Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd /4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.

Reference(s):

1.	Robert L. Boylestad, Louis Nashelsky, ‘‘Electronic Devices and circuit theory”, 11th Edition, Pearson Education, 2017.
2.	Singh M.D and Khanchandani K B, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009.
3.	Umanand L., Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
4.	Dr. Bimbhra P. S., - Power Electronicsll, Khanna Publishers, Delhi, 2012.

*SDG4:Quality Education

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Diodes**	
1.1	PN Junction Diode	1
1.2	Current Voltage Characteristics and Analysis	1
1.3	Diode Logic Gates	1
1.4	Modelling the Diode Forward Characteristics	1
1.5	Graphical Analysis, Small Signal Model	1
1.6	Zener Diode	1
1.7	Varactor Diode	1
1.8	Diode Applications	2
2	**Transistors**	
2.1	Construction and Operation of A Transistor	1
2.2	Input and Output Characteristics of a Transistor in CE Configuration	1
2.3	Operation of CB And CC Configurations	1
2.4	Construction and Characteristics of N Channel JFET	1
2.5	Basic MOSFET Operation	1
2.6	Characteristics of Depletion Type MOSFET	1
2.7	Characteristics of Enhancement Type MOSFET	1
2.8	MOSFET Applications	2
3	**Transducers and Sensors**	
3.1	Classification of Transducers	1
3.2	Transducers Actuating Mechanisms	1
3.3	Resistance Transducers, Variable Inductance Transducers	1
3.4	Capacitive Transducers, Piezoelectric Transducers	1
3.5	Hall Effect Transducers	1
3.6	Noise Introduced by Transducers and Their Reduction	1
3.7	Smart Sensors, Fiber Optic Sensors, MEMS	1
3.8	Ultrasonic Sensors, Applications	2
4	**Optodevices**	
4.1	Introduction	1
4.2	Photo Emitters	1
4.3	Laser	1
4.4	Led	1
4.5	Photoconductive Cell	1
4.6	Opto Coupler	1
4.7	Solid State Relays (Light Operated Relay)	1
4.8	Optical Fibre	2
5	**Power Devices and Convertors**	
5.1	Construction and Operation Of Switching Devices - SCR	2
5.2	MOSFET.	1
5.3	IGBT	1
5.5	Static Characteristics of SCR	1
5.6	Switching Mode Regulators: Buck Regulator	1
5.7	Boost Regulator	1
5.8	Buck-Boost Regulators	1
5.9	Chopper	1

Course Designer(s)

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

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60 GE 002	தமிழரும் தொழில்நுட்பமும் (அனைத்து துறைகளும் பொதுவானது)	Category	L	T	P	Credit
		GE	1	0	0	1*

பாடத்தின் நோக்கங்கள்:

- தமிழர்களின் சங்ககால நெசவு, பானை வனைதல் குறித்து அறிதல்.
- தமிழர்களின் கட்டிடத் தொழில் நுட்பம் குறித்து அறிதல்.
- தமிழர்களின் உற்பத்தி முறைகள் குறித்து அறிதல்.
- தமிழர்களின் சங்ககால வேளாண்மை, நீர்ப்பாசனம் குறித்து கற்றல்.
- நவீன அறிவியல் தமிழ் மற்றும் கணித்தமிழ் குறித்த புரிதல்.

முன்கூட்டிய துறை சார்அறிவு

தேவை இல்லை

பாடம் கற்றதின் விளைவுகள்

பாடத்தை வெற்றிகரமாக கற்றுமுடித்த பின்பு, மாணவர்களால் முடியும் விளைவுகள்

CO1	சங்ககாலத் தமிழர்களின் நெசவு மற்றும் பானை வனைதல் தொழில்நுட்பம் குறித்த கற்றுணர்தல்.	நினைவு கூர்தல், புரிதல்
CO2	சங்ககாலத் தமிழர்களின் கட்டிட தொழில்நுட்பம் கட்டுமானப் பொருட்கள் மற்றும் அவற்றை விளக்கும் தளங்கள் குறித்த அறிவு.	நினைவு கூர்தல், புரிதல்
CO3	சங்ககாலத் தமிழர்களின் உலோகத் தொழில் நாணயங்கள் மற்றும் மணிகள் சார்ந்த தொல்லியல் சான்றுகள் பற்றிய அறிவு.	நினைவு கூர்தல், புரிதல்
CO4	சங்ககாலத் தமிழர்களின் வேளாண்மை, நீர்ப்பாசன முறைகள் மற்றும் முத்து குளித்தல் குறித்த தெளிவு.	நினைவு கூர்தல், புரிதல்
CO5	நவீன அறிவியல் தமிழ் மற்றும் கணித்தமிழ் குறித்த புரிந்துகொள்ளலும் மற்றும் பயன்படுத்துதலும்.	நினைவு கூர்தல், புரிதல், செயல்படுத்துதல்

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	3	3	3	2	-	3	-	-	-
CO2	3	-	-	-	-	-	2	3	2	2	-	3	-	-	-
CO3	3	-	-	-	-	-	3	3	3	2	-	3	-	-	-
CO4	3	-	-	-	-	2	3	3	2	2	-	3	-	-	-
CO5	3	-	-	-	3	-	-	3	-	3	-	3	-	-	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Test (Marks)	End Semester Examination (Marks)
Remember	40	40
Understand	40	40
Apply	20	20
Analysis	-	-
Evaluate	-	-
Create	-	-
Total	100	100

Note: Those who studied Tamil as language subject in +2 should write the exams (Model & End Semester Exams) in Tamil Language only. Those who did not study Tamil as language subject in +2 and other state students can write the exams in English Language. It is mandatory.

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Syllabus

K. S. Rangasamy College of Technology - Autonomous R2022

Common to all Branches

60 GE 002- Tamils and Technology

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	1	0	0	15	1*	40	60	100

Weaving and Ceramic Technology* Weaving Industry during Sangam Age – Ceramic Technology – Black and Red Ware Potteries (BRW) – Graffiti on Potteries.	[3]
Design and Construction Technology* Designing and Structural construction House & Designs in household materials during Sangam Age – Building materials and Hero stones of Sangam age – Details of Stage Constructions in Silappathikaram – Sculptures and Temples of Mamallapuram – Great Temples of Cholas and other worship places – Temples of Nayaka Period - Type Study (Madurai Meenakshi Temple)- Thirumalai Nayakar Mahal – Chetti Nadu Houses , Indo – Saracenic architecture at Madras during British Period.	[3]
Manufacturing Technology* Art of Ship Building – Metallurgical studies – Iron Industry – Iron smelting ,Steel -Copper and gold coins as source of history – Minting of Coins – Beads making – industries Stone beads – Glass beads – Terracotta beads – Shell beads/bone beats – Archeological evidences -Gem stone types described in Silappathikaram.	[3]
Agriculture and Irrigation Technology* Dam,Tank,Ponds,Sluice,Significance of Kumizhi Thoompu of Chola Period,Animal Husbandry – Wells designed for cattle use – Agriculture and Agro Processing – Knowledge of Sea- Fisheries – Pearl – Conche diving -Ancient Knowledge of Ocean – Knowledge Specific Society.	[3]
Scientific Tamil and Tamil Computing* Development of Scientific Tamil – Tamil Computing – Digitalization of Tamil Books – Development of Tamil Software – Tamil Virtual Academy- Tamil Digital Library – Online Tamil Dictionaries – Sorkuvai Project.	[3]
Total Hours:	**15**

Text Book(s):

1.	முனைவர் கே. கே. பிள்ளை, தமிழக வரலாறு - மக்களும் பண்பாடும், தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம், 18th Ed ,2022.
2.	முனைவர் இல. சுந்தரம், கணினித்தமிழ்,விகடன் பிரசுரம், 2nd Ed 2021
3.	முனைவர் இரா.சிவானந்தம், மு.சேரன், கீழடி - வைகை நதிக்கரையில் சங்ககால நகர நாகரிகம், தொல்லியல் துறை வெளியீடு, 6th Ed ,2020.
4.	முனைவர் இரா.சிவானந்தம் , முனைவர் ஜெ.பாஸ்கர், பொருநை - ஆற்றங்கரை நாகரிகம், தொல்லியல் துறை வெளியீடு,1st Ed ,2022
5.	ஈரோடு கதிர் ,உயர்தல் உரிமை ,சிக்ஸ் ப்ளஸ் ஒன் ட்ரெயினிங் அகாடமி st1,Ed,2024
6.	Dr.K.K.Pillay, Social Life of Tamils, TNTB & ESC and RMRL – (In print).
7.	Dr.S.Singaravel, Social Life of the Tamils - The Classical Period, International Institute of Tamil Studies, 1st, 2001.
8.	Dr.S.V.Subaramanian, Dr.K.D. Thirunavukkarasu, Historical Heritage of the Tamils, International Institute of Tamil Studies, 2nd, 2010
9.	Dr.M.Valarmathi, The Contributions of the Tamils to Indian Culture, International Institute of Tamil Studies,
10.	Dr.R.Sivanantham, Keeladi - Sangam City Civilization on the banks of river Vaigai, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation,
11.	Dr.K.K.Pillay, Studies in the History of India with Special Reference to Tamil Nadu, K.K. Pillay(Published by the Author.
12.	Dr.R.Sivanantham, Dr.J.Baskar, Porunai Civilization, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.
13.	R.Balakrishnan, Journey of Civilization Indus to Vaigai, Roja Muthiah Research Library,3rd Ed, 2022

*SDG 4- Quality Education

*For Heritage of Tamils, additional 1 credit is offered and not accounted for CGPA

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K. S. Rangasamy College of Technology - Autonomous R2022

60 GE 002- தமிழரும் தொழில்நுட்பமும்

(அனைத்து துறைகளுக்கும் பொதுவானது)

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	1	0	0	15	1*	40	60	100

நெசவு மற்றும் பானைத் தொழில்நுட்பம்* சங்க காலத்தில் நெசவுத் தொழில் -பானைத் தொழில்நுட்பம் - கருப்பு சிவப்பு பாண்டங்கள் - பாண்டங்களில் கீறல் குறியீடுகள்.	[3]
வடிவமைப்பு மற்றும் கட்டிடத் தொழில்நுட்பம்* சங்க காலத்தில் வடிவமைப்பு மற்றும் கட்டுமானங்கள் & சங்க காலத்தில் வீட்டுப் பொருட்களில் வடிவமைப்பு- சங்க காலத்தில் கட்டுமான பொருட்களும் நடுகல்லும் - சிலப்பதிகாரத்தில் மேடை அமைப்பு பற்றிய விவரங்கள் - மாமல்லபுரச் சிற்பங்களும், கோவில்களும் - சோழர் காலத்துப் பெருங்கோயில்கள் மற்றும் பிற வழிபாட்டுத் தலங்கள் - நாயக்கர் காலக் கோயில்கள் - மாதிரி கட்டமைப்புகள் பற்றி அறிதல், மதுரை மீனாட்சி அம்மன் ஆலயம் மற்றும் திருமலை நாயக்கர் மஹால் - செட்டிநாட்டு வீடுகள் - பிரிட்டிஷ் காலத்தில் சென்னையில் இந்தோ-சாரோசெனிக் கட்டிடக் கலை.	[3]
உற்பத்தித் தொழில் நுட்பம்* கப்பல் கட்டும் கலை - உலோகவியல் -இரும்புத் தொழிற்சாலை - இரும்பை உருக்குதல், எஃகு - - வரலாற்றுச் சான்றுகளாக செம்பு மற்றும் தங்க நாணயங்கள் - நாணயங்கள் அச்சடித்தல் -மணி உருவாக்கும் தொழிற்சாலைகள் - கல்மணிகள், கண்ணாடி மணிகள் - சுடுமண் மணிகள் - சங்கு மணிகள் - எலும்புத்துண்டுகள் - தொல்லியல் சான்றுகள் - சிலப்பதிகாரத்தில் மணிகளின் வகைகள்.	[3]
வேளாண்மை மற்றும் நீர்ப்பாசனத் தொழில் நுட்பம்* அணை, ஏரி, குளங்கள், மதகு - சோழர்காலக் குமுழித் தூம்பின் முக்கியத்துவம் - கால்நடை பராமரிப்பு - கால்நடைகளுக்காக வடிவமைக்கப்பட்ட கிணறுகள் - வேளாண்மை மற்றும் வேளாண்மைச் சார்ந்த செயல்பாடுகள் - கடல்சார் அறிவு - மீன்வளம் - முத்து மற்றும் முத்துக்குளித்தல் - பெருங்கடல் குறித்த பண்டைய அறிவு – அறிவுசார் சமூகம்.	[3]
அறிவியல் தமிழ் மற்றும் கணித்தமிழ்* அறிவியல் தமிழின் வளர்ச்சி - கணித்தமிழ் வளர்ச்சி - தமிழ் நூல்களை மின்பதிப்பு செய்தல் -தமிழ் மென்பொருட்கள் உருவாக்கம் - தமிழ் இணையக் கல்விக்கழகம் - தமிழ் மின் நூலகம் - இணையத்தில் தமிழ் அகராதிகள் - சொற்குவைத் திட்டம்.	[3]
Total Hours:	**15**

Text Book(s):

1.	முனைவர் கே. கே. பிள்ளை, தமிழக வரலாறு - மக்களும் பண்பாடும், தமிழ்நாடு பாடநூல் மற்றும் கல்வியியல் பணிகள் கழகம், 18th Ed ,2022.
2.	முனைவர் இல. சுந்தரம், கணினித்தமிழ்,விகடன் பிரசுரம், 2nd Ed,2021
3.	முனைவர் இரா.சிவானந்தம், மு.சேரன், கீழடி - வைகை நதிக்கரையில் சங்ககால நகர நாகரிகம், தொல்லியல் துறை வெளியீடு, 6th Ed,2020.
4.	முனைவர் இரா.சிவானந்தம் , முனைவர் ஜெ.பாஸ்கர், பொருநை - ஆற்றங்கரை நாகரிகம், தொல்லியல் துறை வெளியீடு,1st Ed ,2022
5.	ஈரோடு கதிர் ,உயர்தல் உரிமை ,சிக்ஸ் ப்ளஸ் ஒன் ட்ரெயினிங் அகாடமி st1,Ed2024,
6.	Dr.K.K.Pillay, Social Life of Tamils, TNTB & ESC and RMRL – (In print).
7.	Dr.S.Singaravel, Social Life of the Tamils - The Classical Period, International Institute of Tamil Studies, 1st, 2001.
8.	Dr.S.V.Subaramanian, Dr.K.D. Thirunavukkarasu, Historical Heritage of the Tamils, International Institute of Tamil Studies, 2nd, 2010
9.	Dr.M.Valarmathi, The Contributions of the Tamils to Indian Culture, International Institute of Tamil Studies,
10.	Dr.R.Sivanantham, Keeladi - Sangam City Civilization on the banks of river Vaigai, Department o Archaeology & Tamil Nadu Text Book and Educational Services Corporation,
11.	Dr.K.K.Pillay, Studies in the History of India with Special Reference to Tamil Nadu, K.K. Pillay(Published by the Author.
12.	Dr.R.Sivanantham, Dr.J.Baskar, Porunai Civilization, Department of Archaeology & Tamil Nadu Text Book and Educational Services Corporation.
13.	R.Balakrishnan, Journey of Civilization Indus to Vaigai, Roja Muthiah Research Library,3rd Ed ,2022

*SDG 4 - Quality Education

* For Heritage of Tamils, additional 1 credit is offered and not accounted for CGPA.

Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 CP 0P2	Engineering Physics and Chemistry Laboratory (CSE, IT, AIML, EEE, ECE, EE)	Category	L	T	P	Credit
		BS	0	0	4	2

Objectives

- To infer the practical knowledge by applying the experimental methods to correlate with the Physics theory.
- To demonstrate an ability to make physical measurements and understand the limits of precision in measurements
- To analyze the behavior and characteristics of various materials for its optimum utilization
- Test the knowledge of theoretical concepts and develop the experimental skills of the learners.
- To facilitate data interpretation and expose the learners to various industrial and environmental applications

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Analyze the properties of semiconducting materials for its potential applications	Apply
CO2	Realize the interference and diffraction phenomena by Airwedge and laser experiments	Apply
CO3	Recognize the magnetic properties by experimental verification	Apply
CO4	Apply different techniques of qualitative and quantitative chemical analysis to generate experimental skills and apply these skills to various analyses	Apply
CO5	Explain and analyze instrumental techniques for chemical analysis	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	-	-	-	-	-	-	2	2	-	-	-	-	-	-
CO2	3	-	-	-	-	-	-	2	2	-	-	-	-	-	-
CO3	3	-	-	-	-	-	-	2	2	-	-	-	-	-	-
CO4	3	-	-	-	-	-	-	2	2	-	-	-	-	-	-
CO5	3	-	-	-	-	-	-	2	2	-	-	-	-	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	10	-	10	10
Understand	30	30	30	30
Apply	40	40	40	40
Analyse	20	30	20	20
Evaluate	-	-	-	-
Create	-	-	-	-
Total	100	100	100	100

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Tiruchengode - 637 215

K.S.Rangasamy College of Technology - Autonomous R2022								
Common to CSE, IT, EEE, ECE, EE								
60 CP 0P2 - Engineering Physics and Chemistry Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	0	0	4	60	2	60	40	100

Physics Laboratory
List of Experiments:**

1. Determination of Hall coefficient of a given semiconductor and its charge carrier density
2. V-I Characteristics of Zener diode and Solar cell
3. Air wedge - Determination of thickness of a thin sheet/wire
4. a) Laser- Determination of the wave length of the laser using grating
   b) Optical fibre -Determination of numerical aperture and acceptance angle
5. Magnetic field along the axis of current carrying coil - Stewart and Gee.

Chemistry Laboratory
List of Experiments*:

1. Estimation of HCl by pH meter.
2. Estimation of mixture of acids by conductivity meter
3. Determination of ferrous ion by Potentiometric titration.
4. Determination of corrosion by weight loss method.
5. Estimation of ferrous ion by spectrophotometer.

Case studies/Activity report

1. Activity using chemdraw software.
2. Activity report on cheminformatic structure.
3. Case study on ion selective electrodes.
4. Assembling of cell or battery.

** SDG 4- Quality Education
* SDG 6 - Improve Clean Water and Sanitation
* SDG 9 - Industry, Innovation, and Infrastructure
* SDG 8 - Decent Work and Economic Growth

Course Designer(s)- Physics

1. Dr. V. Vasudevan - vasudevanv@ksrct.ac.in
2. Mr. S. Vanchinathan - vanchinathan@ksrct.ac.in
3. Dr. P. Suthanthira Kumar - suthanthirakumar@ksrct.ac.in

Course Designer(s)- Chemistry

1. Dr.T.A.Sukantha - sukantha@ksrct.ac.in
2. Dr.B.Srividhya - srividhyab@ksrct.ac.in
3. Dr.K.Prabha - prabhak@ksrct.ac.in
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Chairman - Board of Studies
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60 EV 2P1	Electronic Devices Laboratory	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To analyse the operation of the circuits with diodes in series and parallel combinations
- To design and implement various circuits using diodes
- To design and implement various circuits using BJT& FET
- To analyse the characteristics of various Optical devices
- To implement the application circuits using Power devices

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Analyse the circuits with diodes in series and parallel	Understand
CO2	Implement the application circuits using diodes	Apply
CO3	Implement the application circuits using BJT& FET	Apply
CO4	Analyse the characteristics of optical devices	Understand
CO5	Implement the application circuits using power devices	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	3	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	3	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	-	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	-	3	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	25	-	50	50
Apply	25	25	50	50
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
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K.S.Rangasamy College of Technology - Autonomous R2022								
Common to ECE and EE(VLSIDT)								
60 EV 2P1 - Electronic Devices Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
II	0	0	4	60	2	60	40	100

List of Experiments:

Students have to design application circuits using analog electronic components /MOKU GO Kit/ multisim software

1. *Diode circuit analysis
2. *Application circuits using Diodes***
3. *Application circuits using BJT & FET
4. *Analyse the characteristics of Optical devices
5. *Application circuits using Power devices**

*SDG 4 - Quality Education
** SDG 8 - Descent work and economic growth
***SDG 9 - Industry innovation and infrastructure

Course Designer(s)

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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60 CG 0P1	Career Skill Development - I	Category	L	T	P	Credit
		CG	0	0	2	1*

Objectives

- To help learners improve their vocabulary and to enable them to use words appropriately in different academic and professional contexts
- To help learners develop strategies that could be adopted while reading texts
- To help learners acquire the ability to speak effectively in English in real life and career related situations
- To equip students with effective speaking and listening skills in English
- To facilitate learners to enhance their writing skills with coherence and appropriate format effectively

Pre-requisites

- Basic knowledge of reading and writing in English.

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Listen and comprehend complex academic texts	Understand
CO2	Read and infer the denotative and connotative meanings of technical texts	Analyse
CO3	Write definitions, descriptions, narrations, and essays on various topics	Apply
CO4	Speak fluently and accurately in formal and informal communicative contexts	Apply
CO5	Appraise the verbal ability skills in the career development and professional contexts	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	-	2	3	3	2	3	-	-	-
CO2	-	-	-	-	-	-	-	2	3	3	2	3	-	2	-
CO3	-	-	-	-	-	-	-	2	3	3	2	3	-	2	-
CO4	-	-	-	-	-	-	-	2	3	3	2	3	2	-	-
CO5	-	-	-	-	-	-	-	2	3	3	2	3	2	2	3

3 - Strong; 2 - Medium; 1 - Some

Passed in BoS Meeting held on 13/06/2025
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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

Common to All Branches

60 CG 0P1 - Career Skill Development - I

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
II	0	0	2	30	1*	100	-	100

Listening* Listening for General Information-Specific Details - Audio / Video (Formal & Informal) - Listen to Podcasts/ TED Talks/ Anecdotes / Stories / Event Narration / Documentaries and Interviews with Celebrities - Listen to A Product and Process Descriptions, Advertisements About Products or Services.	[6]
Speaking* Self-Introduction; Introducing A Friend; Conversation - Politeness Strategies - Narrating Personal Experiences / Events; Interviewing A Celebrity; Reporting / And Summarizing of Documentaries / Podcasts/ Interviews - Picture Description; Giving Instruction to Use the Product; Presenting A Product - Small Talk; Mini Presentations - Group Discussions, Debates & Role Plays.	[6]
Reading* Loud Reading Vs Silent Reading, Skimming & Scanning of Passages, Reading Brochures (Technical Context), Social Media Messages Relevant to Technical Contexts and Emails - Biographies, Travelogues, Newspaper Reports and Travel & Technical Blogs - Advertisements, Gadget Reviews and User Manuals - Newspaper Articles and Journal Reports - Editorials; and Opinion Blogs	[6]
Writing* Writing Letters - Informal and Formal - Basics and Format Orientation - Paragraph Texting, Short Report on An Event (Field Trip Etc.) - Definitions; Instructions; and Product /Process Description - Note-Making / Note-Taking; Recommendations; Transferring Information From Non-Verbal (Charts, Graphs To Verbal Mode) - Essay Texting	[6]
Verbal Ability I* Reading Comprehension (Mcqs) - Cloze Test - Sequencing of Sentences - Summarizing and Paraphrase - Error Detection - Spelling Test - Sentence Improvement - Preposition	[6]
Total Hours:	**30**

Reference(s):

1.	"English for Engineers & Technologists" Orient Blackswan Private Ltd. Department of English, Anna University, 2020
2.	Norman Lewis, "Word Power Made Easy - The Complete Handbook for Building a Superior Vocabulary Book", Penguin Random House India, 2020
3.	Michael McCarthy and Felicity O Dell, "English Vocabulary in Use: Upper Intermediate", Cambridge University Press, N.York, 2012
4.	Lakshmi Narayanan, "A Course Book on Technical English", Scitech Publications (India) Pvt. Ltd. 2020.

* SDG 4 - Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Listening**	
1.1	Listening for General Information and Specific Details	1
1.2	Listening to Podcasts, Documentaries and Interviews with Celebrities	1
1.3	Narrating Personal Experiences	1
1.4	Reading Relevant to Technical Contexts and Emails	1
1.5	Listen to A Product and Process Descriptions	2
2	**Speaking**	
2.1	Self-Introduction	1
2.2	Summarizing of Documentaries& Picture Narration	1
2.3	Small Talk; Mini Presentations	1
2.4	Group Discussions, Debates & Role Plays.	1
2.5	Group Discussions	2
3	**Reading**	
3.1	Loud Reading Vs Silent Reading, Skimming & Scanning of Passages	1
3.2	Reading Social Media Messages Relevant to Technical Contexts	1
3.3	Reading Newspaper Reports and Travel & Technical Blogs	1
3.4	Reading Advertisements, Gadget Reviews and User Manuals	1
3.5	Reading Newspaper Articles and Journal Reports	2
4	**Writing**	
4.1	Writing Letters - Informal and Formal	1
4.2	Paragraph Texting	1
4.3	Definitions and Instructions	1
4.4	Note-Making / Note-Taking	1
4.5	Essay Texting	2
5	**Verbal Ability**	
5.1	Reading Comprehension (Mcqs) And Cloze Test	1
5.2	Sequencing of Sentences	1
5.3	Paraphrasing and Summarizing	1
5.4	Error Detection and Spelling Test	1
5.5	Prepositions	2
	Total	**30**

Course Designer(s)

1. Dr.A.Palaniappan - palaniappan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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Tiruchengode - 637 215

K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

THIRD SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 MA 009	Linear Algebra and Numerical Methods	2	40	60	100	45	100
2.	60 CS 002	Data Structures and Algorithms	2	40	60	100	45	100
3.	60 EV 301	Electronic Circuits	2	40	60	100	45	100
4.	60 EV 303	Digital System Design	2	40	60	100	45	100
5.	60 MY 002	Universal Human Values	2	100	-	100	-	100
THEORY CUM PRACTICAL								
6.	60 EV 302	Circuit Analysis	2	50	50	100	45	100
PRACTICAL								
7.	60 EV 3P1	Analog and Digital Electronics Laboratory	3	60	40	100	45	100
8.	61 CS 0P2	Data Structures and Algorithms Laboratory	3	60	40	100	45	100
9.	60 CG 0P2	Career Skill Development – II	1	100	-	100	-	100
10.	60 CG 0P6	Internship	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination, 50 marks for theory cum practical End Semester Examination and 40 marks for practical End Semester Examination.

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Chairman - Board of Studies
Department of Electronics Engineering
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60 MA 009	Linear Algebra and Numerical Methods	Category	L	T	P	Credit
		BS	3	1	0	4

Objectives

- To acquire knowledge about vector spaces.
- To get exposed to the basic concepts of linear transformation
- To know the concepts of interpolation and numerical integration.
- To learn the basics concepts of initial value problems.
- To acquire knowledge of various methods to solve partial differential equations with boundary conditions

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the concept of vector spaces.	Apply
CO2	Interpret the concepts of linear transformation	Apply
CO3	Apply different techniques to find the intermediate values and to evaluate single definite integrals.	Apply
CO4	Compute the solution for initial value problems using single and multi-step methods.	Apply
CO5	Apply various methods to solve partial differential equations with boundary conditions.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO5	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	20
Apply	40	40	70
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

Common to EE & ECE

60 MA 009 – Linear Algebra and Numerical Methods

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	1	0	60	4	40	60	100

Vector Space* Vector Space – Subspace – Null Space – Row and Column Space – Linear Combinations – Linear Independence and Linear Dependence – Basis and Dimension. **Hands – on:** Find a basis and dimension for the vector subspace.	[9]
Linear Transformation and Inner Product Spaces* Linear Transformation – Matrix Representation of a Linear Transformation – Inner Product – Norm – Gram-Schmidt Orthogonalization Process. **Hands – on:** Matrix representation of a linear transformation	[9]
Interpolation and Numerical Integration** Lagrange's and Newton's Divided Difference Interpolation (Unequal Intervals) – Newton's Forward and Backward Interpolation (Equal Intervals) – Two Point and Three Point Gaussian Quadrature – Trapezoidal, Simpson's 1/3 and 3/8 Rule (Single Integral). **Hands – on:** Simpson 1/3 method for definite integral	[9]
Numerical Solution of Ordinary Differential Equations** Single Step Methods: Taylor's Series Method – Euler's Method – Modified Euler's Method- Fourth Order Runge-Kutta Method for Solving First Order Equations – Multi Step Methods: Milne's Predictor and Corrector Method – Adam's Predictor and Corrector Method. **Hands – on:** Runge – Kutta method for solving first order equations.	[9]
Numerical Solution of Partial Differential Equations*** Classifications of Partial Differential Equations of Second Order – Finite Difference Method – Laplace's Equations – Liebmann's Process – Poisson's Equation – Hyperbolic Equation.	[9]
Total Hours: (Lecture – 45; Hands – on – 05; Tutorial – 10)	**60**

Text Book(s):

1.	David C. Lay, "Linear Algebra and its Applications", 6th Edition, Pearson Education, 2022.
2.	Grewal B.S. and Grewal J.S., "Numerical Methods in Engineering and Science", 10th Edition, Khanna Publishers, New Delhi, 2015.

Reference(s):

1.	Howard Anton and Chris Rorres, "Elementary Linear Algebra", 11th Edition, John Wiley & Sons, 2014.
2.	Gilbert Strang, "Linear Algebra and Its Applications", 4th Edition, Brooks/Cole/Cengage, 2006.
3.	Gerald C.F. and Wheatley P.O., "Applied Numerical Analysis", 7th Edition, Pearson Education (Asia), 2007.
4.	Kandasamy P, Thilagavathy K and Gunavathi K, "Numerical Methods", 3rd Edition, S.Chand & CompanyLtd, 2013.

*SDG:4- Quality Education

**SDG:9- Industry, Innovation, and Infrastructure

***SDG:7- Affordable and Clean Energy

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1.0	**Vector Spaces**	
1.1	Vector space	2
1.2	Subspace	1
1.3	Null space, Row and Column space	1
1.4	Linear combinations	2
1.5	Linear independence	1
1.6	linear dependence	1
1.7	Basis and dimension.	1
1.8	Tutorial	2
1.9	Hands on	1
2.0	**Linear Transformation and Inner Product Spaces**	
2.1	Linear transformation	2
2.2	Matrix representation of a linear transformation	1
2.3	Inner product	1
2.4	Problems	1
2.5	Gram-Schmidt orthogonalization process	2
2.6	Problems	2
2.7	Tutorial	2
2.8	Hands on	1
3.0	**Interpolation and Numerical Integration**	
3.1	Lagrange's interpolation	1
3.2	Newton's divided difference Methods	1
3.3	Newton's forward and backward difference Methods.	2
3.4	Two point and three point Gaussian quadratures	2
3.5	Trapezoidal rule	1
3.6	Simpson's1/3 and 3/8 rules	2
3.7	Tutorial	2
3.8	Hands on	1
4.0	**Numerical Solution of Ordinary Differential Equations**	
4.1	Taylor series method	1
4.2	Euler and modified Euler methods	1
4.3	Fourth order Runge – Kutta method	2
4.4	Milne's predictor and corrector methods.	2
4.5	Problems	1
4.6	Adam's predictor and corrector methods.	1
4.7	Problems	1
4.8	Tutorial	2
4.9	Hands on	1
5.0	**Numerical Solution of Partial Differential Equations**	
5.1	Classifications of partial differential equations of second order	1
5.2	Finite difference method	1
5.3	Laplace's equations	2
5.4	Liebmann's process	1
5.5	Poisson's equation	2
5.6	Hyperbolic equation.	1
5.7	Problems	1
5.8	Tutorial	2
5.9	Hands on	1
	Total	60

Course Designer(s)

Mr. D.Senthil Raja – senthilrajad@ksrct.ac.in
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60 CS 002	Data Structures and Algorithms	Category	L	T	P	Credit
		ES	3	0	0	3

Objectives

- To study the asymptotic performance of algorithms and choose the appropriate data structure for a specified application
- To design and implement abstract data types such as linked list, stack, queue and trees
- To learn and implement the hashing techniques
- To design a priority queue adt and its applications
- To demonstrate various sorting, searching and graph algorithms

Pre-requisites

- Nil

Course Outcomes

On the Successful Completion of the Course, Students will be Able to

CO1	Analyse the asymptotic performance of algorithms and express the concept of linear data structures, applications and its implementations	Analyse
CO2	Appraise the knowledge of trees with its operations	Apply
CO3	Recognize the concept of sorting, searching and its types	Apply
CO4	Review various implementations and operations of priority queue, and hashing techniques	Apply
CO5	Apply shortest path and minimum spanning tree algorithms, biconnectivity and algorithmic design paradigms	Analyse

Mapping with Programme Outcomes

Cos	Pos												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	2	2	-	-	2	2	-	-	2	3	3	3
CO2	3	3	2	3	2	-	-	2	3	-	-	2	3	3	3
CO3	3	3	2	2	2	2	-	2	3	2	-	2	3	3	3
CO4	3	3	2	3	2	-	-	3	2	2	-	2	3	3	3
CO5	3	3	2	3	2	2	2	3	3	2	-	2	3	3	3
3 – Strong; 2 – Medium; 1 – Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	10	10	20
Apply	30	40	40
Analyse	10	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E – Electronics Engineering (VLSI Design and Technology)

Common to EE & ECE

60 CS 002 – Data Structures and Algorithms

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Lists, Stacks and Queues Abstraction - Abstract Data Types - Data Representation - Elementary Data Types - Mathematical Preliminaries: Big-Oh Notation - Efficiency of Algorithms - Notion of Time and Space Complexity - Performance Measures for Data Structures - The List ADT - The Stack ADT - The Queue ADT*.	[9]
Trees Preliminaries – Binary Trees – The Search Tree ADT – Binary Search Trees – AVL Trees – Tree Traversals – B–Trees – B+ Trees.	[9]
Sorting and Searching Preliminaries – Insertion Sort – Shell Sort – Heap Sort – Merge Sort – Quick Sort – External Sorting – Searching: Sequential Search - Binary Search – Hashed List Searches	[9]
Hashing and Priority Queues (Heaps) Hashing – Hash Function – Separate Chaining – Open Addressing – Rehashing – Extendible Hashing* – Priority Queues (Heaps) – Model – Simple Implementations – Binary Heap–Applications of Priority Queues – D-Heaps.	[9]
Graphs Definitions – Topological Sort – Shortest-Path Algorithms – Unweighted Shortest Paths – Dijkstra's Algorithm – Minimum Spanning Tree – Prim's Algorithm, Kruskal's Algorithm – Applications of Depth-First Search* – Undirected Graphs – Bi-connectivity. Algorithm Design Paradigms - Greedy, Divide and Conquer, Dynamic Programming, Backtracking	[9]
Total Hours:	45

Text Book(s):	
1.	Weiss M.A., "Data Structures and Algorithm Analysis in C", Second Edition, Pearson Education Asia, 2008.
2.	Langsam Y., Augenstein M.J. and Tenenbaum A.M., "Data Structures Using C", Pearson Education Asia, 2009.
Reference(s):	
1.	Rajesh K.Sukla, "Data Structure Using C & C++", Wiley India, 2012.
2.	Tannenbaum A., "Data Structure Using C", Pearson Education, 2003.
3.	Goodrich and Tamassia, "Data Structures and Algorithms in C++", Second Edition, John Wiley and Sons, 2011
4.	Reema Thareja, "Data Structures Using C", Second Edition, Oxford Higher Education, 2014.

*SDG4 - Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Lists, Stacks and Queues**	
1.1	Abstract Data Type (ADT), Mathematical preliminaries: big-Oh notation	1
1.2	Efficiency of algorithms, Notion of time and space complexity - performance measures for data structures	1
1.3	List ADT	4
1.4	Stack ADT	3
1.5	Queue ADT	3
2	**Trees**	
2.1	Preliminaries	1
2.2	Binary Trees	1
2.3	The Search Tree ADT	1
2.4	Binary Search Trees	1
2.5	AVL Trees	1
2.6	Tree Traversals	1
2.7	B-Trees	2
2.8	B+ Trees	1
3	**Sorting and Searching**	
3.1	Preliminaries, Insertion Sort	1
3.2	Shell Sort, Heap sort	1
3.3	Merge Sort, Quick sort	1
3.4	External Sorting	1
3.5	Sequential Searching	1
3.6	Binary Searching	1
3.7	Hashed List Searches	1
4	**Hashing and Priority Queues (Heaps)**	
4.1	Hashing, Hash Function	1
4.2	Separate Chaining, Open Addressing	1
4.3	Rehashing, Extendible Hashing	1
4.4	Priority Queues (Heaps)	1
4.5	Simple Implementations, Binary Heap	1
4.6	Applications of Priority Queues	1
4.7	d –Heaps	1
5	**Graphs**	
5.1	Graph Definitions - Topological Sort	1
5.2	Shortest-Path Algorithms - Unweighted Shortest Paths	1
5.3	Dijkstra’s Algorithm	1
5.4	Minimum Spanning Tree	1
5.5	Prim’s Algorithm	1
5.6	Kruskal’s Algorithm	1
5.7	Applications of Depth-First Search	1
5.8	Undirected Graphs	1
5.9	Biconnectivity	1
5.10	Algorithm Design Paradigms	1
	Total Hours	**45**

Course Designer(s)

1. Ms.K.Poongodi - poongodik@ksrct.ac.in

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60 EV 301	Electronic Circuits (Common to ECE& EE)	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To understand the operation of different transistor amplifiers
- To design and analyse the feedback amplifiers and oscillators
- To understand the operation of power amplifiers and differential amplifier
- To acquire the basic knowledge of operational amplifier
- To implement application circuits using op-amp.

Pre-requisites

- Electronic Devices

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the operation of different transistor amplifier circuits	Understand
CO2	Describe and analyse the characteristics of negative feedback amplifiers and oscillators	Understand
CO3	Describe the concepts and characteristics of power amplifiers and design differential amplifier	Apply
CO4	Understand the basic concepts of op-amp	Understand
CO5	Design and analyse the various application of op-amp	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	40	60
Apply	-	10	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E - Electronics Engineering (VLSI Design and Technology)

Common to ECE & EE

60 EV 301 - Electronic Circuits

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3	40	60	100

Transistor Amplifiers* Introduction to Biasing Schemes for BJT and FET- Overview of Single Stage BJT Amplifiers: Common Emitter, Common Base, Common Collector- Hybrid-Pi Model -Miller Effect - Frequency Response Of Single Stage MOSFET Amplifier- Cascade and Cascode Amplifiers.	[9]
Feedback Amplifiers and Oscillators * Different Topologies: Voltage Series, Voltage Shunt, Current Series and Current Shunt, Effect on Gain and Frequency Response, Stability Considerations and Frequency Compensation- Basic Concept of Oscillators, RC and LC Sinusoidal Oscillators	[9]
Power Amplifier & Differential Amplifier* Different Modes of Operation of Amplifiers and Their Power Efficiency: Class A, Class B, Class AB and Class C, **Push-Pull Amplifiers and Applications**.** Differential Amplifier: Basic Structure and Principle of Operation - Calculation of Differential Gain, Common Mode Gain, CMRR and ICMR, Design of Differential Amplifier for a Given Specification.	[9]
Basics of Operational Amplifiers* Ideal op-amp Characteristics, General Operational Amplifier Stages and Internal Circuit Diagrams of IC 741, DC Characteristics, AC Characteristics, Frequency Response of Op-Amp, Slew Rate.	[9]
Applications of Operational Amplifiers* Basic Applications of Op-Amp – Inverting and Non-Inverting Amplifiers, Voltage Follower, Scale Changer, Summer, Subtractor, Basic Comparator, **Precision Rectifier, Clipper and Clamper, Peak Detector, V/I & I/V Converters, Switched Capacitor Circuits**: Basic Concept, Practical Configurations**, Application in Amplifier****.	[9]
Total Hours:	45

Text Book(s):

1. David A. Bell, “Electronic Devices and Circuits”, 5th Edition, Oxford University press, 2018.
2. Robert L. Boylestad, Louis Nashelsky, “Electronic Devices and circuit theory”, Pearson Education, 11th Edition, 2017.
3. RoyChoudry D. , Shail Jain , ‘Linear integrated Circuits’, 5th Edition, New Age International Pvt Ltd, 2018.

Reference(s):

1. Anil K. Maini, VarshaAgrawal, “Electronics Devices and Circuits”, Wiley India Pvt.Ltd, 2nd edition, 2019.
2. Salivahanan S., N.Sureshkumar, “Electronic Devices and circuits”, 4th Edition, McGraw-Hill, 2017.
3. Ramakant A., Gayakwad, “Op – Amps and Linear Integrated Circuits”, 4th Edition, Prentice Hall, 2017.

*SDG:4 - Quality Education

**SDG:9 - Industry innovation and infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Transistor Biasing**	
1.1	Introduction to Biasing Schemes for BJT	1
1.2	FET	1
1.3	Overview of Single Stage BJT Amplifiers	1
1.4	Common Emitter Amplifier	1
1.5	Common Base, Common Collector	1
1.6	Hybrid-Pi Model, Miller Effect	1
1.7	Frequency Response of Single Stage MOSFET Amplifier	1
1.8	Cascade Amplifier	1
1.9	Cascode Amplifier	1
2.0	**Feedback Amplifiers and Oscillators**	
2.1	Different Topologies: Voltage Series	1
2.2	Voltage Shunt	1
2.3	Current Series	1
2.4	Current Shunt	1
2.5	Effect on Gain and Frequency Response, Stability Considerations and Frequency Compensation	1
2.6	Basic Concept of Oscillators	1
2.7	RC Oscillators	1
2.8	LC Sinusoidal Oscillators	2
3.0	**Power Amplifier & Differential Amplifier**	
3.1	Different Modes of Operation of Amplifiers	1
3.2	Their Power Efficiency: Class A, Class B,	1
3.3	Class AB and Class C	1
3.4	Push-Pull Amplifiers and Applications	1
3.5	Differential Amplifier: Basic Structure and Principle of Operation	1
3.6	Calculation of Differential Gain, Common Mode Gain, CMRR and ICMR.	1
3.7	Design of Differential Amplifier For a Given Specification	1
4.0	**Basics of Operational Amplifiers**	
4.1	Ideal Op-Amp Characteristics	2
4.2	General Operational Amplifier Stages	
4.3	Internal Circuit Diagrams of IC 741	1
4.4	DC Characteristics	1
4.5	AC Characteristics	2
4.6	Frequency Response of Op-Amp	1
4.7	Slew Rate	1
5.0	**Applications of Operational Amplifiers**	
5.1	Basic Applications of Op-Amp – Inverting and Non-Inverting Amplifiers	1
5.2	Voltage Follower, Scale Changer	1
5.3	Summer, Subtractor	1
5.4	Basic Comparator, Precision Rectifier	
5.5	Clipper and Clamper	1
5.6	Peak Detector	1
5.7	V/I & I/V Converters	1
5.8	Switched Capacitor Circuits: Basic Concept, Practical Configurations	1
5.9	Application in Amplifier	1

Course Designer(s)

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60 EV 302	Circuit Analysis	Category	L	T	P	Credit
		PC	2	1	2	4

Objectives

- To learn the basic concepts and behaviour of DC circuits
- To understand the various network theorems and two port network parameters
- To learn the basic concepts and behaviour of AC circuits
- To understand the transient and steady state response of the circuits subjected to DC excitations and AC with sinusoidal excitations.
- To learn the concept of coupling in circuits and the frequency response of resonant circuits

Pre-requisite:

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the basic laws to analyses the electric circuits using circuit analysis techniques.	Understand
CO2	Apply network theorems and analyse the two-port network behaviour	Apply
CO3	Analyse the steady state response of AC circuits with phasor diagram	Understand
CO4	Apply Laplace Transform for steady state and transient analysis of RC, RL, and RLC networks	Apply
CO5	Analyse the frequency response of electric circuits under resonance and coupled circuits	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	-	3	3	-	2	3	2	3
CO2	3	3	-	-	3	-	-	-	3	3	-	2	3	2	3
CO3	3	3	-	-	2	-	-	-	3	3	-	2	3	2	3
CO4	3	3	-	-	3	-	-	-	3	3	-	2	3	2	3
CO5	3	3	-	-	2	-	-	-	3	3	-	2	3	2	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	10	-	10	-	-	15	-
Understand	10	40	10	40	40	25	40
Apply	40	60	40	60	60	60	60
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 302 - Circuit Analysis

Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	2	1	2	75	4	50	50	100

DC Circuit Analysis* Laws: Ohms Law, Kirchhoff's Current Law, Kirchhoff's Voltage Law, Connections: Sources, Resistors, Inductors And Capacitors In Series and Parallel, Star and Delta Transformations, Voltage, Current Source Conversions. Voltage and Current Division Rules, Nodal Analysis and Mesh Analysis in DC Circuits.	[6]
Network Theorems and Two Port Network* Theorems- Superposition, Thevenin's, Norton's, and Maximum Power Transfer Theorems. Network Parameters - Impedance, Admittance, Transmission and Conversion Formulae.	[6]
Sinusoidal Steady State Analysis * Sinusoidal Steady – State Analysis, Characteristics of Sinusoids, The Phasor, Phasor Relationship For R, L and C, Impedance and Admittance, Phasor Diagrams, AC Circuit Power Analysis, Instantaneous Power, Average Power, Apparent Power and Power Factor, Complex Power, Star and Delta Connections	[6]
Transients* Transient Analysis of RC, RL, And RLC Networks With And Without Initial Conditions With Laplace Transforms Evaluation of Initial Conditions for DC & AC Inputs, State Equations for Networks.	[6]
Resonance and Coupled Circuits* Behavior of Series and Parallel Resonant Circuits, Frequency Response, Quality Factor and Bandwidth. Magnetically Coupled Circuits, Mutual Inductance, Coefficient of Coupling, Dot Rule- Analysis of Coupled Circuits.	[6]
Practical: 1. Measurements of Current and Power of a Specific Branch in a Circuit 2. Measurements of Voltage and Power of a Specific Node in a Circuit 3. Measurement of voltage using mesh analysis 4. Measurement of current using nodal analysis 5. Calculation of various power in an AC circuit 6. Verification of Theorems – Thevenien Theorem -MATLAB 7. Verification of Theorems – Notrons Theorem -MATLAB 8. Verification of Theorems – Superposition Theorem -MATLAB 9. Verification of Theorems – Reciprocity Theorem -MATLAB 10. Check the Transient Response of RL Circuits 11. Check the Transient Response of RC Circuits 12. Check the Transient Response of RLC Circuits	[30]
Total Hours: (Lecture - 30; Practical – 30; Tutorial: 15)	75

Text Book(s):

1.	Sudhakar A and Shyammohan S, "Circuits & Network Analysis and Synthesis", 4th Edition, McGraw Hill, 2021.
2.	Singh R R, "Network Analysis and Synthesis", 2nd Edition, McGraw Hill Education Pvt Limited, 2021.

Reference(s):

1.	Mahmood Nahvi and Joseph Edminister, "Electric Circuits", 6th Edition, Schaum's Outline series, Tata McGraw-Hill, 2014.
2.	William H Hayt& Jack E Kemmerly, "Engineering Circuit Analysis", 8th Edition, McGraw Hill Education, 2013.
3.	Franklin F. Kuo, "Network Analysis and Synthesis", 5th Edition, Wiley International, 2012.
4.	John D Ryder, "Networks, Lines and Fields", 2nd Edition, Pearson Education, 2015.

*SDG: 9 – Quality Education

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**DC Circuit Analysis**	
1.1	Basic Components of Electric Circuits: Charge, Current, Voltage and Power	1
1.2	Voltage and Current Sources. Laws: Ohms Law, Kirchhoff's Current Law, Kirchhoff's Voltage Law,	1
1.3	Voltage and Current Division Rule	1
1.4	Connections: Series and Parallel Connected Sources, Resistors,	1
1.5	Inductor and Capacitor In Series And Parallel Connection	1
1.6	Star and Delta Transformation,	1
1.7	Voltage, Current Sources Conversion.	1
1.8	Nodal Analysis	1
1.9	Mesh Analysis	1
2	**Network Theorems and Two Port Network**	
2.1	Superposition Theorem	1
2.2	Thevenin's Theorem	1
2.3	Norton's Theorem	1
2.4	Maximum Power Transfer Theorems.	1
2.5	Impedance Parameter	1
2.6	Admittance Parameter	1
2.7	Transmission Parameter	1
2.8	Hybrid Parameter	1
2.9	Conversion Formula Between Two Port Parameters	1
3	**Sinusoidal Steady State Analysis**	
3.1	Sinusoidal Steady – State Analysis, Characteristics of Sinusoids	1
3.2	The Phasor Relationship For R, L And C	1
3.3	Impedance and Admittance Diagram	1
3.4	Phasor Diagrams	1
3.5	Ac Circuit Power Analysis	1
3.6	Instantaneous Power, Average Power, Apparent Power and Power Factor, Complex Power	1
3.7	Problems on Various Power	1
3.8	Why Connection	1
3.9	Delta Connection	1
4	**Transients**	
4.1	Transient Analysis of RC Without Initial Conditions	1
4.2	Transient Analysis of RL Without Initial Conditions	1
4.3	Transient Analysis of RLC Networks Without Initial Conditions	2
4.4	Transient Analysis of RC With Initial Conditions	1
4.5	Transient Analysis of RL With Initial Conditions	1
4.6	Transient Analysis of RLC Networks With Initial Conditions	2
4.7	State Equations for Networks.	1
5	**Resonance and Coupled Circuits**	
5.1	Behavior of Series Resonant Circuits, Frequency Response,	1
5.2	Quality Factor and Bandwidth of Series Resonance	1
5.3	Behavior of Parallel Resonant Circuits, Frequency Response	1
5.4	Quality Factor and Bandwidth of Parallel Resonance Circuit	1
5.5	Magnetically Coupled Circuits, Mutual Inductance, Coefficient Of Coupling,	1
5.6	Dot Rule- Analysis of Coupled Circuits.	1
5.7	Introduction to Filters, Classification	1
5.8	T' Filter Network and Its Equation	1
5.9	'Π' Filter Network and Its Equation	1
Practical:		
1.	Measurements of Current and Power of a Specific Branch in a Circuit	3
2.	Measurements of Voltage and Power of a Specific Note in a Circuit	3
3.	Measurement of voltage using mesh analysis	3
4.	Measurement of current using nodal analysis	3
5.	Calculation of various power in an AC circuit	2
6.	Verification of Theorems – Thevenien, Theorem -MATLAB	2

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7.	Verification of Theorems – Notrons, Theorem -MATLAB	2
8.	Verification of Theorems – Superposition Theorem -MATLAB	2
9.	Verification of Theorems – Reciprocity Theorem -MATLAB	2
10.	Check the Transient Response of RL Circuits	3
11.	Check the Transient Response of RC Circuits	3
12.	Check the Transient Response of RLC Circuits	2

Course Designer(s)

1.Dr.S.Pradeep-Pradeeps@ksrct.ac.in

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60 EV 303	Digital System Design (Common to ECE& EE)	Category	L	T	P	Credit
		PC	2	1	0	3

Objectives

- To introduce number systems and codes, basic postulates of Boolean algebra and show the correlation between Boolean expressions.
- To design and analyse combinational circuits
- To study the concept of sequential circuits.
- To introduce the concept of HDL
- Reinforce theory and techniques taught in the classroom through experiments and projects in laboratory

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the fundamentals of numbering system and apply Boolean algebra to design digital systems	Understand
CO2	Design and analyse combinational circuits and semiconductor memories	Apply
CO3	Design and analyse synchronous sequential logic circuits	Apply
CO4	Analyse the asynchronous sequential circuits.	Understand
CO5	Design and verify the digital circuits using HDL.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	-	3	-	-	3	3	3	-	-	3	2	3
CO3	3	3	3	-	3	-	-	3	3	3	-	-	3	2	3
CO4	3	3	-	-	3	-	-	-	-	-	-	-	3	2	-
CO5	2	2	-	-	3	-	-	-	-	-	-	-	3	2	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	20	20	20
Apply	30	30	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

Common to ECE & EE

60 EV 303 - Digital System Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
III	2	1	0	45	3	40	60	100

Digital Fundamentals* Review of Number Systems – Representation-Conversions – Boolean Postulates and Laws – De-Morgan's Theorem – Logic Gates – Minimization of Boolean Expressions – Sum of Products (SoP) – Product of Sums (PoS) – Canonical Forms – Karnaugh Map Minimization – Implementation of Boolean Expressions Using Universal Gates.	[6]
Combinational Circuits* Combinational Logic Circuits – Adders, Subtractors, Decoders, Encoders, Multiplexers, Demultiplexers, Code Convertor, Realization of Boolean Expressions – Using Multiplexers. Memories – ROM Types, RAM Types, PLDs. **Hands - on:** Simulation of Combinational Circuit	[6]
Sequential Circuits* Flip Flops SR, JK, T, D And Master Slave – Characteristic Table and Equation – Flip Flop Conversion, Application Table – Edge Triggering – Level Triggering – Ripple Counters – Synchronous Counters – Modulo – N Counter – **Design of Synchronous FSM – Analysis of Clocked Sequential Circuits*****: State Equation – State Table – State Diagram – State Reduction & Assignment – Register: Shift Registers – Universal Shift Register– Shift Counters **Hands - on:** Simulation of sequential circuit	[6]
Asynchronous Sequential Circuits Analysis Procedure – Transition Table – Flow Table – Race Conditions – Design of Fundamental Mode Circuits – Primitive Flow Table – Reduction of State and Flow Table – Race Free State Assignment – Hazards – Overview and Comparison of Logic Families.	[6]
Introduction to HDL** **Design Flow of VLSI, Different Modelling Styles in Verilog HDL, Structural, Dataflow and Behavioural Modelling of Combinational and Sequential Logic Circuits****	[6]
Total Hours: (Lecture - 30; Tutorial - 15)	45

Text Book(s):	
1.	M. Morris Mano, Michael D. Ciletti, "Digital Design", 5th Edition, Pearson Education, New Delhi, 2016.
2.	Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2016.
Reference(s):	
1.	Anand Kumar, "Fundamentals of Digital Circuits", 4th Edition, Prentice Hall, 2016.
2.	Donald P.Leach and Albert Paul Malvino, GoutamSaha, "Digital Principles and Applications", 8th Edition, Tata McGraw-Hill, New Delhi, 2016.
3.	Salivahanan S. and Arivazhagan S., "Digital Circuits and Design",5th Edition, Oxford University press, 2018.
	John F.Wakerly, "Digital Design: principles and practices", 5th Edition, Pearson Education, 2018.

*SDG:4 - Quality Education

**SDG:8 - Decent work and economic growth

***SDG:9 - Industry,innovation and infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Digital Fundamentals**	
1.1	Review of Number Systems, Conversions, Boolean postulates and laws	1
1.2	Boolean postulates and laws, De-Morgan's Theorem, Logic Gates	1
1.3	Minimization of Boolean expressions	1
1.4	Sum of Products (SOP) – Product of Sums (POS)	1
1.5	Canonical forms- Karnaugh map Minimization	1
1.6	Implementation of Boolean expressions using universal gates.	1
1.7	Tutorial	2
2.0	**Combinational Circuits**	
2.1	Combinational Logic Circuits, Adders, Subtractors,	1
2.2	Decoders, Encoders	1
2.3	Multiplexers, Demultiplexers	1
2.4	Code Convertor	1
2.5	Realization of Boolean Expressions-Using Multiplexers	1
2.6	Memories –ROM types, RAM types, PLDs	1
2.7	Tutorial	2
2.8	Simulation	3
3.0	**Sequential Circuits**	
3.1	Flip flops SR, JK, T, D and Master slave, Characteristic Table and Equation	1
3.2	Flip flop conversion, Application table, Edge triggering – Level Triggering	1
3.3	Ripple counters – Synchronous counters, Modulo – N counter- Design of Synchronous FSM	1
3.4	Analysis of clocked sequential circuits: state equation – State table – State diagram	1
3.5	State reduction & assignment	1
3.6	Register: Shift Registers – Universal Shift Register– Shift counters	1
3.7	Tutorial	2
3.8	Simulation	2
4.0	**Asynchronous Sequential Circuits**	
4.1	Analysis Procedure, Transition Table – Flow Table, Race Conditions	1
4.2	Design of Fundamental Mode Circuits, Primitive Flow Table	1
4.3	Reduction of State and Flow Table, Race Free State Assignment	2
4.4	Hazards	1
4.5	Overview and Comparison of Logic Families	1
4.6	Tutorial	2
5.0	**Introduction to HDL**	
5.1	Design Flow of VLSI	1
5.2	Different Modelling Styles in Verilog HDL,	2
5.3	Structural, Dataflow and Behavioural Modelling of Combinational and Sequential Logic Circuit	3
5.4	Tutorial	2

Course Designer(s)

1. Dr.S.Malarkhodi – malarkhodi@ksrct.ac.in

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60 MY 002	Universal Human Values	Category	L	T	P	Credit
		MC	3	0	0	3#

Objectives

- To identify the essential complementarily between 'values' and 'skills'
- To ensure core aspirations of all human beings.
- To acquire ethical human conduct, trustful and mutually fulfilling human behaviour
- To enrich interaction with Nature
- To achieve holistic perspective towards life and profession

Pre-requisites

- Nil

Course Outcomes

On the Successful Completion of the Course, Students will be Able to

CO1	Discuss the significance of value inputs in formal education and start applying them in their life and profession	Understand
CO2	Evaluate coexistence of the “I” with the body	Analyse
CO3	Identify and evaluate the role of harmony in family, society and universal order	Analyse
CO4	Classify and associate the holistic perception of harmony at all levels of existence and Nature	Analyse
CO5	Develop appropriate human conduct and management patterns to create harmony in professional and personal lives.	Create

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	-	3	2	-	2	3	3	1	1
CO2	-	-	-	-	-	3	-	3	3	-	-	3	3	1	1
CO3	-	-	-	-	-	3	3	3	3	-	-	3	3	1	2
CO4	-	-	-	-	-	3	3	3	3	-	-	3	3	1	2
CO5	-	-	-	-	-	3	3	3	3	3	-	3	3	1	2
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Bloom’s Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	No End Semester Examination
Understand	10	10	
Apply	20	20	
Analyse	20	20	
Evaluate	-	-	
Create	-	-	
Total	60	60	

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 MY 002– Universal Human Values								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
III	3	0	0	45	3#	100	-	100

Introduction to value Education* Understanding Value Education-Self Exploration as the Process for Value Education-Continuous Happiness and Prosperity-The Basic Human Aspirations-Right Understanding-Relationship and Physical Facility –Happiness and Prosperity - Current Scenario – Method to Fulfill the Basic Human Aspirations**	[9]
Harmony in the Human Being* Understanding Human Being as the Co-Existence of the Self and the Body - Distinguishing Between the Needs of the Self and the Body-the Body as an Instrument of the Self-Understanding Harmony In The Self-Harmony of the Self With the Body** – Programme to Ensure Self-Regulation and Health	[9]
Harmony in the Family and Society* Harmony in the Family –The Basic Unit of Human Interaction-Values in Human- to - Human Relationship – 'Trust' The Foundation Value in Relationship – 'Respect'- as the Right Evaluation-Understanding Harmony in The Society –Vision for the Universal Human Order.	[9]
Harmony in the Nature/Existence* Understanding Harmony In The Nature-Interconnectedness, Self-Regulation and Mutual Fulfillment Among the Four Orders of Nature – Realizing Existence as Co-Existence At All Levels –The Holistic Perception of Harmony In Existence.	[9]
Implications of the Holistic Understanding* Natural Acceptance of Human Values- Definitiveness of Human Conduct - A Basis for Humanistic Education, Humanistic Constitution and Universal Human Order - Competence in Professional Ethics – Holistic Technologies, Production Systems and Management Models-Typical Case Studies – Strategies for Transition Towards Value Base Life and Profession	[9]
Total Hours:	45

Text Book(s):	
1.	Gaur R R, Asthana R, Bagaria G P, "A Foundation Course in Human Values and Professional Ethics", 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-87034-47-1.
2.	Gaur R R, Asthana R, Bagaria Teachers G P, "Manual for A Foundation Course in Human Values and Professional Ethics", 2nd Revised Edition, Excel Books, New Delhi, 2019. ISBN 978-93-87034-53-2.
Reference(s):	
1.	Parichaya E K, Nagaraj A, Jeevan Vidya Prakashan, Amarkantak, "Jeevan Vidya" 1999.
2.	Tripathi A.N, "Human Values", New Age International. Publishers, New Delhi, 2004.

*SDG:3 – Good Health and Well-Being
**SDG:5 – Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Introduction to Value Education**	
1.1	Discussion on Present Education System and Skill Based Education	1
1.2	Understanding Value Education	1
1.3	Self-exploration as the process for value education	1
1.4	Basic Human Aspirations - Continuous Happiness and Prosperity	1
1.5	Basic requirements to fulfill Human Aspirations - Right understanding, Relationship and Physical facility	1
1.6	Transformation from Animal Consciousness to Human Consciousness	1
1.7	Sources of Happiness and Prosperity – Harmony and Disharmony	1
1.8	Current Scenario and Role of Education	1
1.9	Outcome of Human Education and Method to fulfill the Basic Human Aspirations	1
2.0	**Harmony in The Human Being**	
2.1	Understanding Human Being - As Co-Existence of The Self and The Body – The Needs of The Self and The Body	1
2.2	Understanding Human Being - As Co-Existence of The Self and The Body - The Activities and Response of The Self and The Body	2
2.3	The Body as An Instrument of The Self	1
2.4	Understanding Harmony in The Self	1
2.5	Harmony of The Self with The Body	2
2.6	Programme To Ensure Self-Regulation and Health	1
2.7	My Participation (Value) Regarding Self and My Body - Correct Appraisal of Our Physical Needs	1
3.0	**Harmony in The Family and Society**	
3.1	Harmony in The Family - Understanding Values in Human Relationships	1
3.2	Family as The Basic Unit of Human Interaction	1
3.3	Values in Human Relationships	1
3.4	Trust - The Foundation Value in Relationship	1
3.5	Respect as The Right Evaluation, The Basis for Respect, Assumed Bases for Respect Today	1
3.6	Harmony from Family to World Family: Undivided Society	1
3.7	Extending Relationship from Family to Society, Identification of The Comprehensive Human Goal	1
3.8	Programs Needed to Achieve the Comprehensive Human Goal: The Five Dimensions of Human Endeavour	1
3.9	Harmony from Family Order to World Family Order – Universal Human Order	1
4.0	**Harmony in The Nature / Existence**	
4.1	The Four Orders in Nature	1
4.2	Participation of Human Being in Entire Nature	1
4.3	Natural Characteristics - Tendency of Human Living with Animal Consciousness / The Holistic Perception of Harmony in Existence	1
4.4	Present Day Problems	1
4.5	Recyclability and Self-Regulation in Nature	1
4.6	Relationship of Mutual Fulfillment	1
4.7	An Introduction to Space, Co-Existence of Units in Space	1
4.8	Harmony in Existence – Understanding Existence as Co- Existence	1
4.9	Natural Characteristic of Human Living with Human Consciousness	1
5.0	**Implications of The Holistic Understanding**	
5.1	Natural Acceptance of Human Values	1
5.2	Definitiveness of Ethical Human Conduct - Development of Human	1

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	Consciousness	
5.3	Identification of Comprehensive Human Goal	1
5.4	Basis for Humanistic Education and Humanistic Constitution	1
5.5	Ensuring Competence in Professional Ethics	1
5.6	Issues in Professional Ethics-The Current Scenario	1
5.7	Holistic Technologies and Production Systems and Management Models - Typical Case Studies	2
5.8	Strategies for Transition Towards Value-Based Life and Profession	1
5.9	Controllability and Observability - Problems	1
	Total	45

Course Designer(s)

1.Dr.G.Vennila - vennila@ksrct.ac.in
2.Dr.K.Raja - rajak@ksrct.ac.in

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60 EV 3P1	Analog and Digital Electronics Laboratory (Common to ECE& EE)	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

To illustrate the working of transistor biasing circuits
To understand and analyse the operation of single stage and multistage amplifiers
To understand and analyse the applications of op-amp
To design and implement combinational and sequential circuits for practical applications
To simulate combinational and sequential circuits using HDL

Pre-requisites

Electronic Devices Laboratory

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design and construct different biasing circuits for BJT & MOSFET	Apply
CO2	Design, implement and obtain the frequency response of single stage CE amplifier and feedback amplifiers.	Apply
CO3	Design and implement an application circuit using power amplifier	Apply
CO4	Design and implement application circuit using combinational and sequential logic circuits	Apply
CO5	Design and simulate combinational and sequential logic circuits using HDL	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO2	3	3	3	-	2	-	-	-	3	3	-	3	3	3	3
CO3	3	3	3	-	2	-	-	-	3	3	-	3	3	3	3
CO4	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO5	2	2	3	-	3	-	-	-	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	10	10	20	20
Apply	40	15	80	80
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 3P1– Analog and Digital Electronics Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
III	0	0	4	60	2	60	40	100

List of Experiments*:

Students have to design application circuits using analog electronic components / MOKU GO Kit / multisim software

Analog experiments*

1. Design and simulation of BJT & MOSFET biasing circuits
2. Design and implementation of MOS amplifier circuits**
3. Analysis of frequency response of feedback amplifiers/ multistage amplifier
4. Design and implementation of application circuits using op-amp**

Digital experiments*

5. Design and implementation of combinational circuits using logic gates**
6. Design and implementation of synchronous sequential circuits**
7. Design and implementation of asynchronous sequential circuits**
8. Design and implementation of FSM (Finite State Machine)**
9. Design and simulation of combinational / synchronous & asynchronous sequential circuits using HDL**

Lab Manual

1.	"Analog and Digital Electronics Laboratory", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG:4- Quality Education

**SDG:9 –Industry innovation and Infrastructure

Course Designer(s)

1. Mrs.S.S.Thamilselvi - sstamilselvi@ksrct.ac.in

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61 CS 0P2	Data Structures and Algorithms Laboratory	Category	L	T	P	Credit
		ES	0	0	4	2

Objectives

- To design and implement simple linear and nonlinear data structures
- To strengthen the ability to identify and apply the suitable data structure for the given real world problem
- To program for storing data as tree structure and implementation of various traversal techniques
- To implement sorting and searching techniques
- To gain knowledge of hashing techniques and graph applications

Pre-requisites

- Programming knowledge in C language

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Demonstrate the implementation of Linear Data structures and its applications	Apply
CO2	Investigate Balanced Parenthesis and Postfix expressions with the help of Stack ADT	Apply
CO3	Implement Non-Linear Data Structure	Apply
CO4	Implement sorting and searching techniques	Apply
CO5	Implement Hashing Techniques, Shortest Path and Minimum Spanning Tree Algorithm	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	-	-	-	-	-	2	-	-	2	3	3	3
CO2	3	3	2	3	-	-	-	-	3	-	-	2	3	3	3
CO3	3	3	2	2	2	2	-	-	3	2	-	2	3	3	3
CO4	3	3	2	3	2	-	-	3	2	2	-	2	3	3	3
CO5	3	3	2	-	2	2	2	3	3	2	-	2	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	-	-
Apply	40	15	80	80
Analyse	10	10	20	20
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
Common to EE & ECE								
61 CS 0P2 - Data Structures and Algorithms Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
III	0	0	4	60	2	60	40	100

List of Experiments*:

1. Implementation of List Abstract Data Type (ADT)*
2. Implementation of Stack ADT*
3. Implementation of Queue ADT*
4. Implementation of stack applications:
   (a) Program for 'Balanced Parenthesis'
   (b) Program for 'Evaluating Postfix Expressions'
5. Implementation Search Tree ADT
6. Implementation of Internal Sorting
7. Develop a program for external sorting
8. Develop a program for various Searching Techniques
9. Implementation of Shortest Path Algorithm*
10. Implementation of Minimum Spanning Tree Algorithm*

Lab Manual

1.	"Data Structures and Algorithms Laboratory", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 9 – Industry Innovation and Infrastructure

Course Designer(s)

1. K.Poongodi - poongodik@ksrct.ac.in

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60 CG 0P2	Career Skill Development II	Category	L	T	P	Credit
		CG	0	0	2	1*

Objectives

- To help learners improve their vocabulary and enable them to use words appropriately in different academic and professional contexts.
- To help learners develop strategies that could be adopted while reading texts.
- To help learners acquire the ability to speak and write effectively in english in real life and career related situations.
- Improve listening, observational skills, and problem-solving capabilities
- Develop message generating and delivery skills

Pre-requisites

- **Nil**

Course Outcomes

On the Successful Completion of the Course, Students will be Able to

CO1	Compare and contrast products and ideas in technical texts	Apply
CO2	Identify cause and effects in events, industrial processes through technical texts	Apply
CO3	Analyse problems in order to arrive at feasible solutions and communicate them orally and in the written format.	Analyse
CO4	Report events and the processes of technical and industrial nature.	Apply
CO5	Articulate their opinions in a planned and logical manner, and draft effective résumés in context of job search.	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	-	-	2	3	3	2	3	2	-	-
CO2	-	-	-	-	-	-	-	2	3	3	2	3	2	-	-
CO3	-	-	-	-	-	-	-	2	3	3	2	3	2	2	2
CO4	-	-	-	-	-	-	-	2	3	3	2	3	-	-	-
CO5	-	-	-	-	-	-	-	2	3	3	2	3	2	2	2
3 - Strong; 2 - Medium; 1 - Some															

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 CG 0P2 - Career Skill Development II								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
III	0	0	2	30	1*	100	00	100

Listening* Evaluative Listening: Advertisements, Product Descriptions, - Audio / Video; Filling A Graphic Organiser (Choosing A Product or Service by Comparison) - Listening to Longer Technical Talks and Completing– Gap Filling Exercises. Listening Technical Information from Podcasts – Listening to Process/Event Descriptions to Identify Cause & Effects, Documentaries Depicting A Technical Problem and Suggesting Solutions - Listening to TED Talks	[6]
Speaking* Marketing A Product, Persuasive Speech Techniques - Describing and Discussing the Reasons of Accidents or Disasters Based on News Reports, Group Discussion (Based on Case Studies), Presenting Oral Reports, Mini Presentations on Select Topics with Visual Aids, Participating in Role Plays, Virtual Interviews	[6]
Reading* Reading Advertisements, User Manuals and Brochures - Longer Technical Texts– Cause and Effect Essays, And Letters / Emails of Complaint - Case Studies, Excerpts from Literary Texts, News Reports Etc. - Company Profiles, Statement of Purpose (Sops)	[6]
Writing* Professional Emails, Email Etiquette - Compare and Contrast Essay - Writing Responses to Complaints Precis Writing, Summarizing and Plagiarism- Job / Internship Application – Cover Letter & Resume	[6]
Verbal Ability II* Reading Comprehension (Inferential Fillups) – Spotting Errors – Verbal Analogies – Theme Detection – Change of Voice – Change of Speech – One Word Substitution	[6]
Total Hours:	**30**
Reference(s):	

1.	"English for Engineers & Technologists", Orient Blackswan Private Ltd. Department of English, Anna University, 2020
2.	Norman Lewis, "Word Power Made Easy - The Complete Handbook for Building a Superior Vocabulary Book", Penguin Random House India, 2020
3.	Raman. Meenakshi, Sharma. Sangeeta, "Professional English". Oxford University Press. New Delhi. 2019
4.	Arthur Brookes and Peter Grundy, "Beginning to Write: Writing Activities for Elementary and Intermediate Learners", Cambridge University Press, New York, 2003

*SDG4 - Quality Education

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Listening**	
1.1	Evaluative Listening: Advertisements, Product Descriptions	1
1.2	Listening to Longer Technical Talks and Completing– Gap Filling Exercises.	1
1.3	Listening Technical Information from Podcasts	1
1.4	Listening to Process/Event Descriptions to Identify Cause & Effects and Documentaries Depicting A Technical Problem and Suggesting Solutions	1
1.5	Listening to TED Talks	2
2.0	**Speaking**	
2.1	Marketing A Product, Persuasive Speech Techniques	1
2.2	Describing and Discussing the Reasons of Accidents or Disasters Based on News Reports,	1
2.3	Group Discussion (Based on Case Studies)	1
2.4	Presenting Oral Reports, Mini Presentations on Select Topics with Visual Aids	1
2.5	Participating in Role Plays and Virtual Interviews	1
3.0	**Reading**	
3.1	Reading Advertisements, User Manuals and Brochures	1
3.2	Reading - Longer Technical Texts– Cause and Effect Essays, and Letters / Emails of Complaint	1
3.3	Case Studies, Excerpts from Literary Texts, News Reports Etc.	1
3.4	Company Profiles	1
3.5	Statement of Purpose (Sops)	2
4.0	**Writing**	
4.1	Professional Emails, Email Etiquette	1
4.2	Compare and Contrast Essay	1
4.3	Writing Responses to Complaints	1
4.4	Precis Writing, Summarizing and Plagiarism	1
4.5	Job / Internship Application – Cover Letter & Resume	2
5.0	**Verbal Ability II**	
5.1	Reading Comprehension (Inferential Fillups) and Theme Detection	1
5.2	Spotting Errors	1
5.3	Verbal Analogies	1
5.4	Change of Voice and Change of Speech	1
5.5	One Word Substitution	2
	Total	**30**

Course Designer(s)

1. Dr.A.Palaniappan - palaniappan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

FOURTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 MA 016	Probability and Inferential Statistics	2	40	60	100	45	100
2.	61 EV 401	Signals and Systems	2	40	60	100	45	100
3.	60 EV 402	Linear Integrated Circuits	2	40	60	100	45	100
4.	60 EV 403	Electromagnetic Waves	2	40	60	100	45	100
5.	60 EV 404	Computer Architecture and Microcontrollers	2	40	60	100	45	100
6.	60 OE L1*	Open Elective I	2	40	60	100	45	100
PRACTICAL								
7.	60 EV 4P1	Linear Integrated Circuits Laboratory	3	60	40	100	45	100
8.	60 EV 4P2	Microcontrollers Laboratory	3	60	40	100	45	100
9.	60 CG 0P3	Career Skill Development – III	1	100	00	100	00	100
10.	60 CG 0P6	Internship	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 for practical End Semester Examination.

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60 MA 016	Probability and Inferential Statistics	Category	L	T	P	Credit
		BS	3	1	0	4

Objectives

- To learn the basic concepts of probability.
- To get exposed to some standard distributions.
- To familiarize the concepts of correlation and regression
- To familiarize various methods in hypothesis testing.
- To get exposed to various statistical methods for time series

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Interpret the basics of probability.	Apply
CO2	Interpret the concepts of standard distributions.	Apply
CO3	Calculate coefficient of correlation and regression.	Apply
CO4	Apply Student's t test, F test and Chi-square test for testing the statistical hypothesis.	Apply
CO5	Apply suitable methods for measuring trend values.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO2	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO3	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
CO5	3	2	-	-	2	-	-	-	-	-	-	-	2	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	20
Apply	40	40	70
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Department of Electronics Engineering
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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 MA 016 - Probability and Inferential Statistics								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
IV	3	1	0	60	4	40	60	100

Probability and Random Variables* Axioms of Probability - Conditional Probability - Baye's Theorem-Random Variable - Expectation - Probability Mass Function - Probability Density Function - Moment Generating Function. **Hands -on:** Calculate the mean and variance for discrete distributions.	[9]
Standard Distributions Discrete Distributions: Binomial, Poisson*** and Geometric Distributions - Continuous Distributions: Uniform, Exponential and Normal Distributions - Properties. **Hands - on:** Fit the Normal distribution.	[9]
Two Dimensional Random Variables* Joint Distributions -Marginal and Conditional Distributions - Covariance - Correlation and Regression - Rank Correlation. **Hands - on:** Calculate the correlation coefficient and lines of regression	[9]
Testing of Hypothesis** Type I and Type II Errors - Test of Significance of Small Samples: Student's 'T' Test -Single Mean - Difference of Means - F- Test - Chi-Square Test - Goodness of Fit - Independence of Attributes. **Hands - on:** Applied Chi-square test to real data set.	[9]
Time Series* Components of a Time Series -Method of Least Square - Parabolic Trend – Exponential Trend - Method of Seasonal Variations - Ratio to Trend Method - Link Relative Method. **Hands - on:** Fit a curve to the given data using method of least squares.	[9]
Total Hours: 45(Lecture) + 5(Hands on) + 10(Tutorial):	**60**

Text Book(s):	
1.	Richard A Johnson, "Miller & Freund's Probability and Statistics for Engineers", 9th Edition, Pearson Education Limited, New Delhi, 2018.
2.	P N Arora and S Arora, ''Statistics for Management'', 5thEdition, Sultan Chand & Sons, New Delhi, 2015.
Reference(s):	
1.	Sheldon Ross, "A first course in Probability", 10thEdition, Pearson Education, New Delhi, 2019.
2.	Veerarajan T., ''Probability, Statistics and Random process'',4th Edition, Tata McGraw-Hill Education, 2015.
3.	Gupta S.P, "Statistical Methods", 45thEdition, Sultan Chand & sons, New Delhi, 2017.
4.	Montgomery D C, Cheryl L.Jennings and Murat Kulahci "Introduction to Time Series Analysis and Forecasting", 2ndEdition, John Wiley and Sons, 2015.

*SDG 4 - Quality Education
**SDG 9 - Industry, Innovation, and Infrastructure
***SDG 2 - Zero Hunger

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Probability and Random Variables**	
1.1	Axioms of Probability	1
1.2	Conditional Probability	1
1.3	Baye''S Theorem	2
1.4	Tutorial	2
1.5	Random Variable, Expectation	1
1.6	Probability Mass Function	1
1.7	Probability Density Function	1
1.8	Moments Generating Function.	1
1.9	Tutorial	2
2	**Standard Distributions**	
2.1	Discrete Distributions- Binomial Distribution	2
2.2	Poisson Distribution	1
2.3	Geometric Distribution	1
2.4	Tutorial	2
2.5	Continuous Distributions - Uniform Distribution	1
2.6	Exponential Distribution	1
2.7	Normal Distribution	2
2.8	Properties	1
2.9	Tutorial	2
3	**Two Dimensional Random Variables**	
3.1	Joint Distributions	1
3.2	Marginal Distribution	1
3.3	Conditional Distribution	1
3.4	Tutorial	2
3.5	Covariance	1
3.6	Correlation	1
3.7	Regression	2
3.8	Rank Correlation	1
3.9	Tutorial	2
4	**Testing of Hypothesis**	
4.1	Type I And Type II Errors	1
4.2	Test of Significance of Small Samples -Student's 'T' Test	1
4.3	Single Mean	1
4.4	Difference of Means.	2
4.5	Tutorial	2
4.6	F- Test	1
4.7	Chi-Square Test - Goodness of Fit	1
4.8	Independence of Attributes.	1
4.9	Tutorial	2
5	**Time Series**	
5.1	Components of A Time Series	1
5.2	Method of Least Square	1
5.3	Parabolic Trend	2
5.4	Exponential Trend	1
5.5	Tutorial	2
5.6	Method of Seasonal Variations	1
5.7	Ratio to Trend Method	1
5.8	Link Relative Method	1
5.9	Tutorial	2

Course Designer(s)

1 Mrs. D.Padmavathi - padmavathi@ksrct.ac.in
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61 EV 401	Signals and Systems	Category	L	T	P	Credit
		PC	2	1	0	3

Objectives

- To understand and perform operations on continuous-time and discrete-time signals and analyze LTI systems using convolution.
- To analyze continuous-time signals and systems using Continuous Time Fourier Transform (CTFT).
- To study sampling and analyze discrete-time signals using Discrete Time Fourier Transform (DTFT).
- To apply Z-transform for solving discrete-time system equations and studying stability.
- To understand and implement DFT and FFT algorithms for frequency analysis.

Pre-requisites

- Integrals, Partial Differential Equations and Laplace transform.

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Classify signals and systems and analyze LTI systems using convolution techniques.	Apply
CO2	Analyze continuous-time signals and systems in the frequency domain using CTFT.	Apply
CO3	Analyze discrete-time signals and systems in the frequency domain using DTFT.	Apply
CO4	Analyze discrete-time signals and systems using Z-transform.	Apply
CO5	Perform efficient frequency analysis using DFT and FFT algorithms.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	-	-	-	3	3	3	2
CO2	3	3	-	-	3	-	-	3	-	-	-	3	3	3	2
CO3	3	3	-	-	3	-	-	3	-	-	-	3	3	3	2
CO4	3	3	-	-	3	-	-	3	3	-	3	3	3	3	2
CO5	3	3	-	-	3	-	-	3	-	-	-	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	30
Apply	40	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

B.E - Electronics Engineering (VLSI Design and Technology)

61 EV 401 - Signals and Systems

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
IV	2	1	0	45	3	40	60	100

Introduction to Signals and Systems* Basic Continuous Time (CT) & Discrete Time (DT) Signals - Classification of CT & DT Signals - Signal Operations - Classification-Properties of CT & DT Systems - Analysis of LTI Systems- Convolution Sum-Convolution Integral -Properties. **Hands - On:** Signal generation & operations and verification of system properties	[6]
Fourier Analysis of Continuous Time Signals and Systems* Periodic Signal Representation by Trigonometric Fourier series- Representation of CT Aperiodic and Periodic Signals by Continuous Time Fourier Transform - Properties - Frequency Response of Systems Characterized by Differential Equations. **Hands - On:** Analysis of CT Signals and Systems Using Fourier Transform	[6]
Fourier Analysis of Discrete Time Signals and Systems* Sampling: Sampling Theorem, Signal Reconstruction-Representation of DT Aperiodic and Periodic Signals by Discrete Time Fourier Transform - Properties - Frequency Response of Systems Characterized by Difference Equations. **Hands - On:** Analysis of DT Signals and Systems Using Fourier Transform	[6]
Z Transform Analysis of Discrete Time Signals and Systems* Z Transform - Two Sided and One-Sided Z Transform - Properties of Z Transform - Properties of ROC - Inverse Z Transform, Analysis of LTI Systems Using Z Transform - Stability and Causality in Z-Domain - Frequency Response of Systems Characterized by Difference Equations. **Hands - On:** Analysis of DT Systems Using Z-Transform.	[6]
DFT and FFT Algorithms* Introduction - Frequency Domain Sampling: Discrete Fourier Transform (DFT) - Properties of DFT - Efficient Computation of the DFT: FFT Algorithms - Radix 2 FFT Algorithms: Decimation in Time and Decimation in Frequency. **Hands - On:** Verification of Properties of DFT	[6]
Total Hours: (Lecture - 30; Tutorial - 15):	45

Text Book(s):

1. Alan V.Oppenheim, Alan S.Willsky with Hamid Nawab S., ‘‘Signals & Systems’‘, 2nd Edition, Pearson Education, 2013.
2. B P Lathi, ‘‘Signal processing and Linear systems”, Oxford University Press, 2010.

Reference(s):

1. John G.Proakis and Dimitris G.Manolakis, ‘‘Digital Signal Processing, Principles, Algorithms and Applications”, 4th Edition, Prentice Hall, 2013.
2. Roberts M.J., ‘‘Signals and Systems Analysis using Transform method and MATLAB”, 3rd Edition, Tata McGraw-Hill, 2018.
3. Simon Haykin and Barry Van Veen, ‘‘Signals and Systems”, 2nd Edition, John Wiley & Sons, 2012

*SDG 4 - Quality Education

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Introduction to signals and systems**	
1.1	Basic Continuous-Time (Ct) & Discrete-Time (DT) Signals	1
1.2	Classification of CT Signals and DT Signals	1
1.3	Signal Operations, Classification	1
1.4	Properties of CT Systems and DT Systems	1
1.5	Analysis of LTI Systems: Convolution Sum	1
1.6	Convolution Integral, Properties	1
1.7	Hands on	1
1.8	Tutorial	2
2	**Fourier Analysis of Continuous Time Signals and Systems**	
2.1	Periodic Signal Representation by Trigonometric Fourier series	1
2.2	Representation of CT Aperiodic Signals by Continuous Time Fourier Transform	1
2.3	Representation of CT Periodic Signals by Continuous Time Fourier Transform	1
2.4	Properties	1
2.5	Frequency Response of Systems Characterized by Differential Equations	2
2.6	Hands on	1
2.7	Tutorial	2
3	**Fourier Analysis of Discrete Time Signals and Systems**	
3.1	Sampling: Sampling Theorem	1
3.2	Signal Reconstruction	1
3.3	Representation of DT Aperiodic Signals by Discrete Time Fourier Transform	1
3.4	Representation of DT Periodic Signals by Discrete Time Fourier Transform	1
3.5	Properties	1
3.6	Frequency Response of Systems Characterized by Difference Equations	1
3.7	Hands on	1
3.8	Tutorial	2
4	**Z Transform Analysis of Discrete Time Signals and Systems**	
4.1	Z Transform - Two Sided and One-Sided Z Transform	1
4.2	Properties of Z Transform and Properties of ROC	1
4.3	Inverse Z Transform	1
4.4	Analysis of LTI Systems Using Z Transform	1
4.5	Stability and Causality In Z-Domain	1
4.6	Frequency Response of Systems Characterized by Difference Equations.	1
4.7	Hands on	1
4.8	Tutorial	2
5	**DFT And FFT Algorithms**	
5.1	Frequency Domain Sampling	1
5.2	Discrete Fourier Transform (DFT)& Properties of DFT	2
5.4	Efficient Computation of the DFT: FFT Algorithms	1
5.5	Radix 2 FFT Algorithms: Decimation in Time	1
5.6	Radix 2 FFT Algorithms: Decimation in Frequency	1
5.7	Hands on	1
5.8	Tutorial	2

Course Designer(s)

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60 EV 402	Linear Integrated Circuits (Common to ECE & EE)	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

To study the circuit configuration of linear integrated circuits.
To introduce practical applications of linear integrated circuits.
To introduce the concept of analog multiplier and Phase Locked Loop with applications.
To study the application of ADC and DAC in real time systems.
To introduce special function ICs and its construction.

Pre-requisites

Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the circuit configuration of linear integrated circuits.	Understand
CO2	Design linear and non-linear circuits using op-amps	Apply
CO3	Explain the operation and applications of analog multiplier and PLL	Understand
CO4	Design ADC and DAC circuits using op-amps	Apply
CO5	Explain the working principle of special function ICs	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	-	3	3	3		-	3	3	-
CO2	2	2	3	3	3	-	-	-	-	-	-	3	3	3	-
CO3	2	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	3	3	3	-	-	3	3	3		3	3	3	3
CO5	3	3	3	3	3	-	-	-	-	-	-	3	3	3	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	25	25	40
Apply	25	25	40
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 402 - Linear Integrated Circuits

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
IV	3	0	0	45	3	40	60	100

Circuit Configuration for Linear ICs* Current Sources, Analysis of Differential Amplifiers with Active Loads, Supply and Temperature Independent Biasing, Band Gap References, Monolithic IC Operational Amplifiers, Specifications, Frequency Compensation, Slew Rate and Methods of Improving Slew Rate. Interpretation of TL082 Datasheet. **Hands - On:** Design And Simulation Of Differential Amplifier	[9]
Linear and Non-Linear Applications of Op-Amp* Linear and Nonlinear Circuits Using Operational Amplifiers and Their Analysis, Differentiator, Integrator, Instrumentation Amplifier, Sine Wave Oscillators, Low Pass, High Pass and Band Pass Filters, Multivibrator And Schmitt Trigger, Triangle Wave Generator, Log and Antilog Amplifiers. **Hands - On:** Design and Simulation of Differentiator	[9]
Analog Multiplier and PLL* Analysis of Four Quadrants and Variable Transconductance Multipliers, Analog Multiplier MPY634 Features, Voltage Controlled Oscillator, Closed Loop Analysis of PLL, AM, PM and FSK Modulators and Demodulators.	[9]
Analog to Digital and Digital to Analog Convertors * Sample and Hold Circuit -Digital to Analog Converters - Binary Weighted and R-2R Ladder Types - Analog to Digital Converters - Flash - Counter Ramp, Successive Approximation, Single, Dual Slope - DAC/ADC Performance Characteristics and Comparison. **Hands - On:** AD/DA Converters	[9]
Special Function ICs 555 Timers, Voltage Regulators - Linear and Switched Mode Types, Switched Capacitor Filter, SMPS, Frequency to Voltage Converters, Power Amplifiers and Isolation Amplifiers, Sources for Noises, Op-Amp Noise Analysis and Low Noise Op-Amps. **	[9]
Total Hours:	45

Text Book(s):

1.	RoyChoudry D., Shail Jain , ‘‘Linear integrated Circuits’‘, 5th Edition, New Age International Pvt Ltd, 2018.
2.	Ramakant A., Gayakwad, ‘‘Op - Amps and Linear Integrated Circuits’‘, 4th Edition, Prentice Hall, 2017.

Reference(s):

1.	Sergio Franco, "Design with Operational Amplifiers and Analog Integrated Circuits", Mc Graw Hill Education, 2014.
2.	Sergio Franco., ‘‘Design with Operational Amplifiers and Analog Integrated Circuits’‘, 4th Edition, Tata McGraw-Hill, 2014.
3.	Salivahanan S. & V.S. KanchanaBhaskaran, ‘‘Linear Integrated Circuits’‘, 3rd Edition, TMH, 2018.
4.	Gray and Meyer, ‘‘Analysis and Design of Analog Integrated Circuits’‘, 5th Edition, Wiley International, 2010.

*SDG 4 - Quality Education

**SDG 9 - Industry, Innovation and Infrastructure

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**Circuit Configuration for Linear ICs:**	
1.1	Current Sources	2
1.2	Analysis of Difference Amplifiers with Active Loads	2
1.3	Supply and Temperature Independent Biasing	1
1.4	Monolithic IC Operational Amplifiers, Specifications	1
1.5	Frequency Compensation	1
1.6	Slew Rate and Methods of Improving Slew Rate.	1
1.7	Interpretation of TL082 Datasheet	1
2	**Application of Operational Amplifiers**	
2.1	Differentiator, Integrator	1
2.2	Instrumentation Amplifier	1
2.3	Sine Wave Oscillators	2
2.4	Low Pass, High Pass And	1
2.5	Band Pass Filters	
2.6	Schmitt Trigger	1
2.7	Multivibrator, Triangle Wave Generator	1
2.8	Log and Antilog Amplifiers.	1
3	**Analog Multiplier And PLL**	
3.1	Analysis of Four Quadrants and Variable Transconductance Multipliers	2
3.2	Analog Multiplier MPY634 Features	1
3.3	Voltage Controlled Oscillator	1
3.4	Closed Loop Analysis Of PLL	2
3.5	AM, PM Modulators and Demodulators	2
3.6	FSK Modulators and Demodulators	1
4	**Analog to Digital and Digital to Analog Convertors**	
4.1	Digital to Analog Converters - Binary Weighted	1
4.2	Digital to Analog Converters - R-2R Ladder Types	1
4.3	Sample and Hold Circuit	2
4.4	Continuous - Counter Ramp Type ADC	1
4.5	Successive Approximation	1
4.6	Single, Dual Slope	2
4.7	DAC/ADC Performance Characteristics and Comparison.	1
5	**Special Function ICs**	
5.1	555 Timers	2
5.2	Voltage Regulators - Linear and Switched Mode Types	1
5.3	Voltage Regulators -Switched Capacitor Filter	1
5.4	SMPS	1
5.5	Frequency to Voltage Converters	1
5.6	Power Amplifiers and Isolation Amplifiers	1
5.7	Op Amp Noise Analysis	1
5.8	Low Noise OP-Amps	1

Course Designer(s)

1. Mr.D.Poornakumar - poornakumard@ksrct.ac.in

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60 EV 403	Electromagnetic Waves	Category	L	T	P	Credit
		PC	2	1	0	3

Objectives

- To introduce the concept of vector analysis
- To develop an understanding of electromagnetic laws and its application in boundaries
- To study maxwell's equation, plane wave propagation in free space
- To introduce the concept of signal propagation through transmission lines and high frequency lines
- To illustrate the propagation of TE, TM and TEM rectangular, circular waveguides and cavity resonators

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the vector quantities and apply vector integration and differentiation in different coordinate systems	Apply
CO2	Apply the laws of electromagnetic to evaluate the boundary conditions for electric and magnetic fields and describe the propagation of plane electromagnetic waves	Apply
CO3	Apply Faraday's law to find the electromotive force and Calculate displacement current using Maxwell's equation for time varying magnetic field	Apply
CO4	Evaluate the characteristics and wave propagation in high frequency transmission lines	Apply
CO5	Describe rectangular and circular waveguides and understand the propagation of electromagnetic waves	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	2	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	-	-	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	-	-	-	-	3	3	3	-	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	30
Understand	20	20	30
Apply	30	30	40
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 403 - Electromagnetic Waves

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
IV	2	1	0	45	3	40	60	100

Vector Analysis * Vectors Analysis: Vector Algebra, Vector Calculus - Divergence, Gradient, Curl, Laplacian; Coordinate Systems - Cartesian, Cylindrical **Hands - On:** 1. Generate Electromagnetic Wave	[6]
Electromagnetics * Coulomb's Law, Gauss's Law, Electric Scalar Potential, Laplace and Poisson's Equations, Boundary Conditions, Biot-Savart Law, Ampere's Law **Hands - On:** Solve a 2-D Magnetostatic Model for a Ferromagnetic Frame with an H-Shaped Cavity	[6]
Electrodynamics* Maxwell's Equations, Faraday's Induction, Displacement Current, Plane Wave Propagation in Free Space and In Materials; Poynting Vector	[6]
Transmission Lines* Transmission-Line General Solution - Loading. Impedance Transformation and Matching. Smith Chart, Quarter-Wave Transformers. Single Stub Matching	[6]
Waveguides* Classification of Guided Wave Solutions-TE and TM Waves. Rectangular and Circular Waveguides. Excitation of Waveguides. Rectangular Cavity Resonators	[6]
Total Hours: (Lecture - 30; Tutorial - 15)	**45**

Text Book(s):	
1.	Matthew N.O.Sadiku , "Elements of Electromagnetics", 7th Edition , Oxford University Press , 2018.
2.	Jordan E.C. & Balmain K.G., "Electromagnetic waves & Radiating Systems", 2nd Edition, Prentice Hall, 2013.
Reference(s):	
1.	William H.Hayt, John A.Buck , "Engineering Electromagnetics", 8th Edition, McGraw Hill Education, 2017.
2.	John. D. Ryder, "Network Lines and Fields", 2nd Edition, Pearson Education India, 2015.
3.	David K.Cheng, "Field and Wave Electromagnetics", 2nd Edition, Pearson Education, 2015.
4.	Umesh Sinha, "Transmission Lines and Networks", Satya Prakashan Publishing Company, New Delhi, 2010.

*****SDG 4 - Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Vector Analysis**	
1.1	Vectors, Position & Distance Vector, Component of Vectors	1
1.2	Cartesian and Cylindrical Coordinate Systems	1
1.3	Vector Calculus-Differential Length, Area, Volume	1
1.4	Line, Surface & Volume Integrals - Del Operator	1
1.5	Gradient of Scalar-Divergence of a Vector & Divergence Theorem-Curl of a Vector	1
1.6	Stokes Theorem- Laplacian of Scalar and Vector Field	1
2.0	**Electromagnetics**	
2.1	Coulomb's Law	1
2.2	Gauss's Law	1
2.3	Electric Scalar Potential	1
2.4	Laplace and Poisson's Equations	1
2.5	Boundary Conditions	1
2.6	Biot-Savart Law & Ampere's Law	1
3.0	**Electrodynamics**	
3.1	Maxwell's Equations	2
3.2	Faraday's Induction	1
3.3	Displacement Current	1
3.4	Plane Wave Propagation in Free Space and In Materials	1
3.5	Poynting Vector	1
4.0	**Transmission Lines**	
4.1	Transmission Line - V & I Equation of Transmission Line	1
4.2	Propagation Constant & Characteristic Impedance	1
4.3	Reflection Coefficient & VSWR	1
4.4	Impedance Transformation and Matching & Quarter-Wave Transformers	1
4.5	Smith Chart	1
4.6	Single Stub Matching	1
5.0	**Waveguides**	
5.1	Classification of Waveguides	1
5.2	TM Waves in Rectangular Waveguides	1
5.3	TE Waves in Rectangular Waveguides	1
5.4	Characteristics of TE, TM Waves	1
5.5	TM and TE Waves in Circular Waveguides & Excitation of Waveguides	1
5.6	Rectangular Cavity Resonators	1

Course Designer(s)

Mr.D.Poornakumar-Poornakumard@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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60 EV 404	Computer Architecture and Microcontrollers	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To learn in detail the different types of control and the concept of pipelining,
- Learn the hierarchical memory system including cache memories and virtual memory.
- To introduce the architecture, programming of 8051 micro controller
- Interfacing an peripheral device with the 8051 microcontroller
- To explore the applications using microcontroller 8051

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Acquire the knowledge of fundamentals of different types of control and the concept of pipelining	Understand
CO2	Discuss the operation of different I/O systems and Memory devices	Understand
CO3	Describe the operation of 8051 microcontroller and develop the assembly language program using 8051 microcontrollers	Understand
CO4	Do interfacing design of peripherals like Timers and Standard interfaces	Apply
CO5	Develop the 8051-microcontroller based system for various applications	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	3	-	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	-	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	3	-	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	50	30	60
Apply	-	20	30
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design & Technology)

60 EV 404 - Computer Architecture and Microcontrollers

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
IV	3	0	0	45	3	40	60	100

Computer Organization and Architecture* Architecture, Structure and Function. Computer Components, Function, and Bus Interconnection. Instruction Sets Characteristics and Functions, Addressing Modes, Stack Operation, RISC - CISC, And Pipelining Principles.	[9]
Computer Memory Systems* Memory Access Characteristics, Memory Hierarchy, Cache Memory Improving Cache Performance. Virtual Memory - Overlay, Memory Management, Address Translation. Input/Output Organization - Introduction, Synchronous Vs. Asynchronous I/O, Programmed I/O, Interrupt Driven I/O, Direct Memory Access	[9]
8051 Architecture* Microcontrollers and Embedded Processors. Architecture - Block Diagram of 8051, Working Registers, SFRS, Clock and Reset Circuits, Stack and Stack Pointer, Program Counter, I/O Ports, Memory Structures, Data and Program Memory, Timing Diagrams and Execution Cycles. 8051 Instruction Set, Addressing Modes, Instruction Timings, Data Transfer Instructions, Arithmetic Instructions, Logical Instructions, Branch Instructions, Subroutine Instructions, Bit Manipulation Instruction	[9]
Instruction Set and Programming* Assembly Language Programs, C Language Programs. Programming on Timer, Interrupt and Serial Data Transfer. Assemblers and Compilers. Programming and Debugging Tools. Standard Interfaces - RS232, RS485, USB, SPI And I2C.	[9]
Programming and Interfacing of 8051* Interfacing of Sensors, DAC, ADC, PWM, Keypad, Seven Segments LED Display. DC Motor, LED, Stepper Motor and LCD Interfacing	[9]
Total Hours:	**45**

Text Book(s):	
1.	Muhammed Ali Mazidi& Janice GilliMazidi, R.D. Kinley, The 8051 microcontrollers
2.	Subrata Ghoshal, Computer Architecture and Organization: From 8085 to Core2Duo and beyond, Pearson, 2011.
Reference(s):	
1.	Mano M M, Computer System Architecture, 3rd Ed, Prentice Hall of India.
2.	Computer organization and design: The Hardware/Software interface/David A.
3.	Computer Organisation V. Carl Hamacher, Zvonko G. Vranesic, SafwatG.Zaky.
4.	John P Hayes, Computer Architecture and Organization, McGraw Hill.

*SDG:9 - Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Computer Organization and Architecture**	
1.1	Architecture, Structure and Function	1
1.2	Computer Components, Function	1
1.3	Bus Interconnection	1
1.4	Instruction Sets	1
1.5	Characteristics and Functions	1
1.6	Addressing Modes	1
1.7	Stack Operation	1
1.8	RISC-CISC	1
1.9	Pipelining Principles	1
2.0	**Computer Memory Systems**	
2.1	Memory Access Characteristics	1
2.2	Memory Hierarchy	1
2.3	Cache Memory Improving Cache Performance	1
2.4	Virtual Memory - Overlay	1
2.5	Memory Management	1
2.6	Address Translation. Input/Output Organization	1
2.7	Introduction, Synchronous Vs. Asynchronous I/O, Programmed I/O	1
2.8	Interrupt Driven I/O	1
2.9	Direct Memory Access	1
3.0	**8051 Architecture**	
3.1	Microcontrollers and Embedded Processors	1
3.2	Architecture - Block Diagram Of 8051, Clock and RESET Circuits	1
3.3	Working Registers, SFRS	1
3.4	Stack and Stack Pointer, Program Counter, I/O Ports	1
3.5	Memory Structures, Data and Program Memory	1
3.6	Timing Diagrams and Execution Cycles	1
3.7	8051 Instruction Set	1
3.8	Addressing Modes	1
3.9	Instruction Timings, Data Transfer Instructions, Arithmetic Instructions, Logical Instructions, Branch Instructions, Subroutine Instructions, Bit Manipulation Instruction.	1
4.0	**Instruction Set and Programming**	
4.1	Assembly Language Programs	1
4.2	C Language Programs. Programming on Timer	1
4.3	Programming on Interrupt	1
4.4	Programming on Serial Data Transfer	1
4.5	Assemblers and Compilers	1
4.6	Programming and Debugging Tools	1
4.7	Standard Interfaces - RS232, RS485	1
4.8	Standard Interfaces- USB, SPI	1
4.9	Standard Interfaces- I^2C	1
5.0	**Programming and Interfacing Of 8051**	
5.1	Interfacing of Sensors	1
5.2	DAC, ADC	1
5.3	PWM	1
5.4	Keypad	1
5.5	Led	1
5.6	Seven Segments Led Display	1
5.7	Dc Motor	1
5.8	Stepper Motor	1
5.9	LCD Interfacing	1

Course Designer(s)

1. Dr.S.Gomathi-gomathi@ksrct.ac.in

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60 EV 4P1	Linear Integrated Circuits Laboratory	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To design and test the various circuits using Op-amp
- To design and test the various circuits using 555 timer
- To construct and test the phase locked loop
- To construct and test different data convertor circuits
- To demonstrate DC Power supply using LM317 and LM723

Pre-requisites

- Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design and test the various applications of op-amp	Apply
CO2	Design and test the various applications of NE555 timer	Apply
CO3	Design and test the various applications of PLL	Apply
CO4	Design and test the different data convertors	Apply
CO5	Design and Test DC Power supply using LM317 and LM723	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	3	-	-	3	3	-	3	3	3	3
CO2	3	3	3	-	3	3	-	-	3	3	-	3	3	3	3
CO3	3	3	3	-	3	3	-	-	3	3	-	3	3	3	3
CO4	3	3	3	-	3	3	-	-	3	3	-	3	3	3	3
CO5	3	3	3	-	3	2	-	-	3	3	-	-	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	20	20
Apply	50	25	80	80
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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K.S.Rangasamy College of Technology - Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 4P1- Linear Integrated Circuits Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
IV	0	0	4	60	2	60	40	100

List of Experiments*:

1.Design and test an Instrumentation amplifier
2.Design and test an Active Low pass and Band pass filters
3.Design and test a Waveform Generators using op-amp - Astable and Monostable
4.Design and test a Phase shift and Wien bridge oscillators using op-amp
5. Application circuits using Op-Amp

6.Design and test an Astable and Monostable multivibrator using NE555 Timer
7.Study the Characteristics of PLL
8.Design and test a Data converters-ADC & DAC
9.DC power supply using LM317 and LM723
10. Application circuits using NE555 timer

Lab Manual	
1.	"Linear Integrated Circuits Laboratory" Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 4 - Quality Education

Course Designer(s)

1. Mr D.Poornakumar - poornakumard@ksrct.ac.in

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60 EV 4P2	Microcontrollers Laboratory	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To equip students with the ability to perform arithmetic and logical operations using the 8051 microcontroller.
- To develop proficiency in using assembly language programming to solve real-world computational tasks.
- To provide hands-on experience in interfacing peripheral devices like motors, DACs, and counters with the 8051 microcontroller.
- To introduce waveform generation techniques using digital-to-analog conversion and microcontroller programming.
- To enhance the students' problem-solving skills by implementing Boolean expressions and code conversion algorithms

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Demonstrate arithmetic and logical operations using the 8051 microcontroller in assembly language.	Apply
CO2	Realize Boolean expressions and counters using the 8051 microcontroller.	Apply
CO3	Perform code conversion and wave form generation using 8051 microcontroller.	Apply
CO4	Interface and control electromechanical devices through the 8051 microcontroller.	Apply
CO5	Write efficient assembly language programs for advanced microcontroller applications using KEIL software.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	2	3	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	20	10	30	30
Apply	30	15	70	70
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
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B.E. Electronics Engineering (VLSI Design and Technology)								
60 EV 4P2 - Microcontrollers Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
IV	0	0	4	60	2	60	40	100

List of Experiments*:

1. Arithmetic Operations using 8051 microcontroller
2. Finding largest and smallest number in the given array using 8051 microcontroller
3. Realization of Boolean expressions using 8051 microcontroller
4. Counter using 8051 microcontroller
5. Code conversion using 8051 microcontroller
6. Waveform generation using DAC with 8051 microcontroller
7. Interfacing and programming of stepper motor and DC motor control with 8051
8. Write an assembly language program for generating square waveform using KEIL software (AT89C51)
9. Write an assembly language program for multibyte addition using KEIL software (AT89C51)
10. Write an assembly language program for arranging in ascending/descending order using KEIL software (AT89C51)

Lab Manual

1.	"Microcontrollers Lab manual" Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG:9 - Industry Innovation and Infrastructure

Course Designer(s)

1. Dr.S.Gomathi - gomathi@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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Tiruchengode - 637 215

60 CG 0P3	Career Skill Development - III	Category	L	T	P	Credit
		CG	0	0	2	1*

Objectives

- To help learners improve their logical reasoning skills at different academic and professional contexts.
- To help learners relate basic quantitative problems and solve them.
- To help learners Infer critically the statements with optimal conclusions and assumptions.
- To Solve the quantitative problems pertaining to calculations of averages, ratio and proportions, and profit and loss effectively
- To compute quantitative problems related to time and work, speed and distance, and simple and compound interest

Pre-requisites

- Basic knowledge of Arithmetic and Logical Reasoning

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Deduce the topics in logical reasoning at the preliminary and intermediate level.	Analyse
CO2	Relate basic quantitative problems and solve them effectively at the preliminary level	Apply
CO3	Infer critically the statements with optimal conclusions and assumptions with the data and information given.	Analyse
CO4	Solve the quantitative problems pertaining to calculations of averages, ratio and proportions, and profit and loss effectively at the pre-intermediate level.	Apply
CO5	Compute quantitative problems related to time and work, speed and distance, and simple and compound interest at intermediate level.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2	2	2	3	-	3	-	-	-	2	3	3	2	3	3
CO2	3	3	3	3	-	2	-	-	-	2	3	3	2	3	3
CO3	2	2	2	2	-	3	-	-	-	2	3	3	2	3	3
CO4	3	3	3	3	-	2	-	-	-	2	3	3	2	3	3
CO5	3	3	3	3	-	2	-	-	-	2	3	3	2	3	3
3 - Strong; 2 - Medium; 1 - Some															

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022								
Common to All Branches								
60 CG 0P3 - Career Skill Development - III								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
IV	0	0	2	30	1*	100	-	100

Logical Reasoning* Analogies - Alpha and Numeric Series - Number Series - Coding and Decoding - Blood Relations - Coded Relations - Order and Ranking - Odd Man Out - Direction and Distance	[6]
Quantitative Aptitude - Part 1* Number System - Squares & Cubes - Divisibility - Unit Digits - Remainder Theorem - HCF & Lcm - Geometric and Arithmetic Progression - Surds & Indices	[6]
Critical Reasoning* Syllogism - Statements and Conclusions, Cause and Effect, Statements and Assumptions - Identifying Strong Arguments and Weak Arguments - Cause and Action - Data Sufficiency	[6]
Quantitative Aptitude - Part 2* Average - Ratio and Proportion - Ages - Partnership- Percentage - Profit & Loss -Discount - Mixture and Allegation	[6]
Quantitative Aptitude - Part 3* Time & Work - Pipes and Cistern - Time, Speed & Distance - Trains - Boats and Streams - Simple Interest and Compound Interest	[6]
Total Hours:	30

Reference(s):

1.	Aggarwal, R.S. “A Modern Approach to Verbal and Non-verbal Reasoning”, Revised Edition 2008, Reprint 2009, S.Chand & Co Ltd., New Delhi.
2.	Abhijit Guha, “Quantitative Aptitude”, 6th Edition, McGraw Hill Education, 2016.
3.	Dinesh Khattar, “Quantitative Aptitude for Competitive Examinations”, Pearson Education 2020.
4.	Anne Thomson, “Critical Reasoning: A Practical Introductio”, 3rd Edition, Lexicon Books, 2022.

*SDG 4 - Quality Education
*SDG 8 - Decent work and Economic growth
*SDG 9 - Industry, innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Logical Reasoning**	
1.1	Analogies - Alpha and Numeric Series	1
1.2	Number Series - Coding and Decoding	1
1.3	Blood Relations - Coded Relations	1
1.4	Order and Ranking - Odd Man Out	1
1.5	Direction and Distance	2
2.0	**Quantitative Aptitude - Part 1**	
2.1	Number System	1
2.2	Squares & Cubes - Divisibility	1
2.3	Unit Digits - Remainder Theorem	1
2.4	HCF & LCM- Geometric and Arithmetic Progression	1
2.5	Surds & Indices	2
3.0	**Critical Reasoning**	
3.1	Syllogism	1
3.2	Statements and Conclusions, Cause and Effect	1
3.3	Statements and Assumptions	1
3.4	Identifying Strong Arguments and Weak Arguments	1
3.5	Cause and Action -Data Sufficiency	2
4.0	**Quantitative Aptitude - Part 2**	
4.1	Average - Ratio and Proportion	1
4.2	Ages - Partnership	1
4.3	Percentage	1
4.4	Profit & Loss	1
4.5	Discount - Mixture and Allegation	2
5.0	**Quantitative Aptitude - Part 3**	
5.1	Time & Work	1
5.2	Pipes and Cistern	1
5.3	Time, Speed & Distance - Trains	1
5.4	Boats and Streams	1
5.5	Simple Interest and Compound Interest	2

Course Designer(s)

1. R. Poovarasan - poovarasan@ksrct.ac.in

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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS

(For the candidates admitted in 2025-2026)

FIFTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EV 501	Control Systems Engineering	2	40	60	100	45	100
2.	60 EV 502	VLSI and Chip Design	2	40	60	100	45	100
3.	60 EV 503	Digital Signal Processing	2	40	60	100	45	100
4.	60 EV E1*	Professional Elective I	2	40	60	100	45	100
5.	60 OE L2*	Open Elective II	2	40	60	100	45	100
THEORY CUM PRACTICAL								
6.	60 EV 504	Machine Learning in VLSI System Design	2	50	50	100	45	100
PRACTICAL								
7.	60 EV 5P1	VLSI Laboratory	3	60	40	100	45	100
8.	60 EV 5P2	Signal Processing Laboratory	3	60	40	100	45	100
9.	60 EV 5P3	Design Thinking and Innovation Laboratory	3	60	40	100	45	100
10.	60 CG 0P4	Career Skill Development IV	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination, 50 marks for theory cum practical End Semester Examination and 40 marks for practical End Semester Examination.

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60 EV 501	Control Systems Engineering	Category	L	T	P	Credit
		PC	3	1	0	4

Objectives

- To understand the concepts of mathematical models, transfer function, block diagram reduction techniques and signal flow graphs.
- To learn methods for improving system time response and frequency response and types of controllers.
- To learn the concepts of stability in time domain and frequency domain.
- To analyse the frequency domain response of the given systems.
- To analyse digital control system using the state space technique

Pre-requisites

- Integrals, Partial Differential Equations and Laplace Transform

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Derive the mathematical modelling of the physical systems and find out the transfer function using block diagram reduction techniques and signal flow graphs.	Apply
CO2	Apply standard test signals to a second order control system to determine their characteristics in time and frequency domain.	Apply
CO3	Analyse the control system behaviour using stability analysis technique.	Apply
CO4	Analyse the open loop control system using frequency response methods and various types of compensators to determine stability margins.	Apply
CO5	Analyse the state variable model of a discrete time control systems.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	2	-	-	-	3	3	-	-	3	2	3
CO2	3	3	3	-	2	-	-	-	3	3	-	-	3	2	3
CO3	3	3	3	-	2	-	-	-	3	3	-	-	3	2	3
CO4	3	3	3	-	2	-	-	-	3	3	-	-	3	2	3
CO5	3	3	3	-	2	-	-	-	3	3	-	-	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	10	10	30
Apply	40	40	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 501 - Control Systems Engineering

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	1	0	60	4	40	60	100

Systems Modeling* Basic elements in control systems - Open loop and Closed loop Systems – Transfer function - Modeling of Electrical and Mechanical Systems - Translational and Rotational Systems - Block Diagram Reduction Techniques - Signal Flow Graph - Mason's Gain Formula - Applications of Control Systems - Drone Control System Design****.** **Hands on:** Write a Program to Find the Overall Transfer Function if the Two System are Connected to Cascade System, Parallel System and Feedback System.	[9]
Time and Frequency Domain Analysis* Standard Test Signals - Time Response of First and Second Order Systems - Performance Specifications on System Time Response - Steady State Error - Introduction to PID Controllers - Performance Specifications on System Frequency Response. **Hands on:** Plot the Time Response and Frequency Response of the Given System Subjected to Standard inputs	[9]
Stability Analysis* Concepts of Stability – Characteristics equation - Routh Stability Criterion - Concepts of Root Locus Technique - Guidelines for Sketching Root Locus. **Hands on**: Sketch the Root Locus of the Unity Feedback Systems Governed by the Open Loop Transfer Function	[9]
Frequency Response and System Analysis* Bode plot - Polar plot - Nyquist stability Criterion - Compensator Design using Bode Plot - Cascade Lead Compensation, Cascade Lag Compensation. **Hands on:** Write a Program to Draw the Polar Plot and Bode Plot for Various Open Loop Transfer Function and Calculate Gain Margin and Phase Margin.	[9]
State Space Analysis of Digital Control Systems* State Space Representation of DiscreteTtime Systems - Solution of Discrete Time State Space Equation - State Transition Matrix - Decomposition Techniques - Controllability and Observability, **Hands on:** Write a Program to Determine the Controllability and Observability of the System Governed by State Model.	[9]
Total Hours: (Lecture - 45; Tutorial - 15)	**60**

Text Book(s):

1.	Gopal M., "Control Systems, Principles & Design", 4th Edition, Tata McGraw Hill, 2012.
2.	Nagrath I.J. & Gopal M., "Control Systems Engineering", 6th Edition, New Age International Publishers, 2018.

Reference(s):

1.	Norman S.Nise, "Control Systems Engineering", 8th Edition, Wiley, 2019.
2.	Ogata K., "Modern Control Engineering", 5th Edition, Pearson Education India, 2015.
3.	Benjamin.C. Kuo, Farid Golnaraghi, "Automatic Control Systems", 10th Edition, McGraw-Hill Education, 2017.
4.	Smarajit Ghosh, "Control systems: Theory and applications", 2nd Edition, Pearson Education India, 2013.

*SDG: 4- Quality Education

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(VLSI Design and Technology)
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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Systems Modeling**	
1.1	Basic elements in control systems, Open Loop and Closed Loop Systems & Modeling of Electrical Systems	1
1.2	Transfer Function,Modeling of Mechanical Systems	1
1.3	Translational Systems	1
1.4	Rotational Systems	1
1.5	Block Diagram Reduction - Rules	1
1.6	Block Diagram Reduction Techniques	1
1.7	Signal Flow Graph - Concept	1
1.8	Mason's Gain Formula - Problem	1
1.9	Applications of Control Systems - Drone Control System Design	1
	Tutorial	2
2.0	**Time and Frequency Domain Analysis**	
2.1	Standard Test Signals	1
2.2	Time Response of First and Second Order Systems	1
2.3	Time Response of Second Order Systems- Problems	1
2.4	Performance Specifications on System Time Response- Concepts	1
2.5	Performance Specifications on System Time Response- Problems	1
2.6	Types of Systems & Steady State Error	1
2.7	Introduction to PID Controllers	1
2.8	Performance Specifications on System Frequency Response	1
2.9	Specifications on System Frequency Response - Problems	1
	Tutorial	2
3.0	**Stability Analysis**	
3.1	Concepts of Stability-Characteristics Equation	1
3.2	Routh Stability Criterion - Concepts	1
3.3	Routh Stability Criterion - Problems	1
3.4	Routh Stability Criterion - Problems	1
3.5	Concepts of Root Locus Technique	1
3.6	Guidelines for Sketching Root Locus	1
3.7	Sketching Root Locus	1
3.8	Sketch the Root Locus - Problems	1
3.9	Sketch the Root Locus - Problems	1
	Tutorial	2
4.0	**Frequency Response and System Analysis**	
4.1	Polar Plot	1
4.2	Nyquist Stability Criterion	1
4.3	Bode Plot - Concepts	1
4.4	Bode Plot - Problems	1
4.5	Compensator Design Using Bode Plot - Concepts	1
4.6	Cascade Lead Compensation - Procedure	1
4.7	Cascade Lead Compensation - Problems	1
4.8	Cascade Lag Compensation - Procedure	1
4.9	Cascade Lag Compensation - Problems	1
	Tutorial	2
5.0	**State Space Analysis of Digital Control Systems**	
5.1	State Space Representation of Discrete Time Systems	1
5.2	Solution of Discrete Time State Space Equation - Concepts	1
5.3	Solution of Discrete Time State Space Equation - Problems	1
5.4	State Transition Matrix - Concepts	1
5.5	State Transition Matrix - Problems	1
5.6	Decomposition Techniques	1
5.7	Decomposition Techniques - Problems	1
5.8	Controllability and Observability - Concepts	1
5.9	Controllability and Observability - Problems	1
	Tutorial	1

Course Designer(s)

1. Dr.S.Gomathi-gomathi@ksrct.ac.in

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60 EV 502	VLSI and Chip Design	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To study the fundamentals of IC technology components and their characteristics.
- To understand the combinational logic circuits and design principles.
- To understand sequential logic circuits and clocking strategies.
- To know the arithmetic building blocks and memory architecture.
- To learn the concept of testability and ASIC Design of VLSI circuits.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the fundamental principles of MOS transistor and fabrication technologies in VLSI design.	Apply
CO2	Describe combinational logic circuits and design principles	Understand
CO3	Describe sequential logic circuits and clocking strategies	Understand
CO4	Design arithmetic building blocks and memory architecture	Apply
CO5	Illustrate the ASIC design process and testing principles	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	40	40	60
Apply	10	10	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 502 - VLSI and Chip Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

MOS Transistor Principles* Long Channel I-V Characteristics - VTC Parameters (DC Characteristics) - Second Order Effects - CMOS Logic - CMOS Fabrication: n-Well Processes - Layout Design Rules -Stick Diagrams - Advanced Technologies*: FinFET, RibbonFET.	[9]
Combinational Logic Circuits Propagation Delays - Elmore's Constant - Power Dissipation - Low Power Design Principles - Static CMOS Design - Dynamic CMOS Design.	[9]
Sequential Logic Circuits and Clocking Strategies Static Latches and Registers - Dynamic Latches and Registers - Pipelines - Non-Bistable Sequential Circuits - Timing Classification of Digital Systems - Synchronous Design - Self Timed Circuit Design.	[9]
Arithmetic Building Blocks and Memory Architecture* Adders – Multipliers - Shift Registers - Logic Implementation using Programmable Devices (ROM, PLA, FPGA) - Memory Architecture and Building Blocks - Memory Core and Memory Peripherals Circuitry*.	[9]
ASIC Design and Testing Principles ASIC Design Flow - ASIC Types: Full Custom, Semi-Custom, FPGA – Testing Principles: Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles: Fault Models, Automatic Test Pattern Generation.	[9]
Total Hours:	45

Text Book(s):

1. Jan M Rabaey, Anantha Chandrakasan, "Digital Integrated Circuits: A Design Perspective", PHI, 2016
2. Neil H E Weste, Kamran Eshranghian, "Principles of CMOS VLSI Design: A System Perspective", Addison Wesley, 2017

Reference(s):

1. Smith M.J., "Application Specific Integrated Circuits", Addison Wesley, 2002
2. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2011
3. Charles H Roth Jr, Lizy Kurian John and Byeong Kil Lee, "Digital Systems Design using Verilog", 1st Edition, Cengage Learning, 2016
4. Parag K.Lala," Digital Circuit Testing and Testability", Academic Press, 1997

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**MOS Transistor Principles**	
1.1	Long channel I-V characteristics	1
1.2	VTC Parameters (DC characteristics)	1
1.3	Second Order Effects	1
1.4	CMOS Logic	1
1.5	CMOS Fabrication: n-Well Processes	1
1.6	Layout Design Rules	1
1.7	Technology Scaling	1
1.8	Advanced Technologies: FinFET,	1
1.9	Advanced Technologies: RibbonFET	1
2.0	**Combinational Logic Circuits**	
2.1	Propagation Delays	1
2.2	Elmore's Constant	1
2.3	Power Dissipation	1
2.4	Low Power Design Principles	1
2.5	Static CMOS Design: Complementary CMOS	1
2.6	Static CMOS Design: Ratioed Logic	1
2.7	Static CMOS Design: Pass-Transistor Logic	1
2.8	Dynamic CMOS Design: Basic Principles, Speed and Power Dissipation of Dynamic Logic	1
2.9	Dynamic CMOS Design: Issues in Dynamic Design	1
3.0	**Sequential Logic Circuits and Clocking Strategies**	
3.1	Static Latches and Registers	1
3.2	Dynamic Latches and Registers	1
3.3	Pipelines	1
3.4	Non-Bistable Sequential Circuits: The Schmitt Trigger	1
3.5	Non-Bistable Sequential Circuits: Monostable Sequential Circuits	1
3.6	Non-Bistable Sequential Circuits: Astable Circuits	1
3.7	Timing Classification of Digital Systems	1
3.8	Synchronous Design	1
3.9	Self-Timed Circuit Design	1
4.0	**Arithmetic Building Blocks and Memory Architecture**	
4.1	Adders	1
4.2	Multipliers	1
4.3	Shift Registers	1
4.4	Logic Implementation using Programmable Devices (ROM, PLA)	1
4.5	Logic Implementation using Programmable Devices (FPGA)	1
4.6	Memory Architecture	1
4.7	Memory Building Blocks	1
4.8	Memory core	1
4.9	Memory peripherals circuitry	1
5.0	**ASIC Design and Design for Testability**	
5.1	ASIC Design Flow	1
5.2	ASIC Types: Full Custom, Semi-Custom	1
5.3	FPGA	2
5.4	Issues in Design for Testability	1
5.5	Fault Model Types: Stuck-At-0	1
5.6	Fault Model Types: Stuck-At-1	1
5.7	Automatic Test Pattern Generation	2

Course Designer(s)

1. Mrs.C.Saranya - saranyac@ksrct.ac.in

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60 EV 503	Digital Signal Processing	Category	L	T	P	Credit
		PC	3	1	0	4

Objectives

- To design and analyze DSP system FIR and IIR filters
- To study the fundamentals of multi rate filters
- To study the basic of adaptive filters
- To understand finite word length effects
- To study digital signal processors systems for given specifications and applications

Pre-requisites

- Signals and Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design IIR filters using Impulse Invariant and Bilinear Transformation Techniques.	Apply
CO2	Design linear phase FIR filters using Windowing Techniques and sampling method.	Apply
CO3	Apply the concept of sampling rate conversation and adaptive filters in DSP applications.	Apply
CO4	Analyse the effects of Finite word length on digital filters.	Apply
CO5	Describe the architecture of TMS320C6x DSP processor.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	3	-	-	3	3	2	2
CO2	3	3	3	-	3	-	-	-	3	-	-	3	3	2	2
CO3	3	3	3	-	3	-	-	-	3	-	-	3	3	2	2
CO4	3	3	3	-	-	-	-	-	3	-	-	3	3	2	2
CO5	3	3	-	-	3	-	-	-	3	-	-	3	3	2	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	20	20	30
Apply	30	30	50
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K.S.Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 503 - Digital Signal Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	1	0	60	4	40	60	100

Design of IIR Filters* Design of IIR Filters from Analog Filters - Frequency Transformation - IIR Filters (Butterworth): Properties- Design: Impulse Invariant Technique - Bilinear Transformation - Realization of IIR filters.	[9]
Design of FIR Filters* Design of FIR Filters - Symmetric and Anti symmetric FIR Filters - Design of Linear Phase FIR Filters: Windowing Techniques (Rectangular, Hamming, Hanning) - Frequency Sampling - Realization of FIR Filters.	[9]
Multirate Signal Processing* Multirate Operations - Decimation and Interpolation - Fractional Sampling Rate Alteration - Interconnection of Building Blocks -The Noble Identities - The Poly Phase Representation - Efficient Structure of Decimation and Interpolation Filters - Concepts of Adaptive Filter - FIR Adaptive Filters - LMS Algorithm.	[9]
Finite Word Length Effects* Representation of Numbers - Fixed Point and Floating Point Representation - Errors Resulting From Rounding and Truncation - Quantization Process and Error- Analysis of Coefficient Quantization Effects - A/D Conversion Noise Analysis - Quantization Noise Model - Signal to Quantization Noise Ratio - Round off Effects in Digital Filters - Limit Cycle Oscillations in Recursive Systems - Scaling to Prevent Overflow.	[9]
Digital Signal Processors* Programmable DSPs - TMS320C6X DSPs, Architectures Features - DSP Building Blocks- Memory Space Organization - External Bus Interfacing Signals - Memory Interface - Parallel I/O Interface- Programmed I/O - Interrupts and I/O -Direct Memory Access (DMA).	[9]
Total Hours: (Lecture - 45; Tutorial - 15)	**60**

Text Book(s):

1.	John G Proakis, Dimitris G Manolakis, "Digital Signal Processing Principles, Algorithms and Application", 4th Edition, Pearson, 2014.
2.	Venkataramani B. & Bhaskar M., "Digital Signal Processor Architecture, Programming and Application", 2nd Edition, McGraw-Hill, 2014.

Reference(s):

1.	Mitra S.K., "Digital Signal Processing: A Computer based approach", Fourth Edition, McGraw Hill, 2013.
2.	Alan V Oppenheim, Ronald W Schafer, John R Back, "Discrete Time Signal Processing", 3rd Edition, Pearson, 2013.
3.	Monson H.Hayes, "Statistical Digital Signal Processing and Modelling", John Wiley & Sons, 2013.
4.	Thad B. Welch, Cameron H.G. Wright, Michael G. Morrow, "Real-Time Digital Signal Processing from MATLAB to C with the TMS320C6x DSPs", CRC Press, 2016.

*SDG 9 - Industry Innovation and Infrastructure

Course Contents and Lecture Schedule

S. No.	Topics	No. of

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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		hours
1.0	**Design of IIR Filters**	
1.1	Design of IIR Filters From Analog Filters	1
1.2	Frequency Transformation (Low pass to high pass)	1
1.3	Frequency Transformation (Low pass to band pass)	1
1.4	IIR Filters (Butterworth): Properties	1
1.5	Impulse Invariant Technique	1
1.6	Bilinear Transformation	1
1.7	Design of Butterworth filter with Impulse Invariant Technique	1
1.8	Design of Butterworth filter with Bilinear Transformation	1
1.9	Realization of IIR Filters	1
	Tutorial	4
2.0	**Design of FIR Filters**	
2.1	Design of FIR Filters	1
2.2	Symmetric	1
2.3	Anti-symmetric FIR Filters	1
2.4	Design of Linear Phase FIR Filters	1
2.5	Windowing Techniques - Rectangular	1
2.6	Windowing Techniques - Hamming	1
2.7	Windowing Techniques - Hanning	1
2.8	Frequency Sampling & Realization of FIR Filters	2
	Tutorial	4
3.0	**Multirate Signal Processing**	
3.1	Multirate Operations - Decimation and Interpolation	1
3.2	Fractional Sampling Rate Alteration	1
3.3	Interconnection of Building Blocks	1
3.4	The Noble Identities	1
3.5	The Poly Phase Representation	1
3.6	Efficient Structure of Decimation and Interpolation Filters	1
3.7	Concepts of Adaptive Filter	1
3.8	FIR Adaptive Filters	1
3.9	LMS Algorithm	1
	Tutorial	2
4.0	**Finite Word Length Effects**	
4.1	Representation of Numbers - Fixed Point and Floating Point Representation	1
4.2	Errors Resulting from Rounding and Truncation	1
4.3	Quantization Process and Error	1
4.4	Analysis of Coefficient Quantization Effects	1
4.5	A/D Conversion Noise Analysis	1
4.6	Quantization Noise Model	1
4.7	Signal to Quantization Noise Ratio	1
4.8	Round off Effects in Digital Filters	1
4.9	Limit Cycle Oscillations in Recursive Systems - Scaling to Prevent Overflow	1
	Tutorial	4
5.0	**Digital Signal Processors**	
5.1	Programmable DSPs - TMS320C6X DSPs	1
5.2	Architectures Features	1
5.3	DSP Building Blocks	1
5.4	Memory Space Organization	1
5.5	External Bus Interfacing Signals	1
5.6	Memory Interface - Parallel I/O Interface, Programmed I/O	1
5.7	Interrupts and I/O & Direct Memory Access (DMA)	2
	Tutorial	1
Course Designer(s)		
1. Mr.S.Pradeep-pradeeps@ksrct.ac.in		

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60 EV 504	Machine Learning in VLSI System Design	Category	L	T	P	Credit
		PC	2	0	2	3

Objectives

- To introduce the fundamentals of machine learning architecture and its applications in modern computing systems.
- To explore the mathematical modeling of artificial neurons and neural network architectures, including single-layer and multilayer feed-forward networks.
- To provide an in-depth understanding of supervised and unsupervised learning techniques, including advanced algorithms like backpropagation and support vector machines.
- To study VLSI implementation techniques for neural networks, focusing on efficient hardware design strategies.
- To analyze deep neural network architectures, their key components, and the optimization of hardware accelerators for improved performance.

Pre-requisites

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the mathematical models for artificial neurons and design basic neural network architectures.	Understand
CO2	Apply supervised and unsupervised learning algorithms to solve classification and clustering problems.	Apply
CO3	Design and optimize VLSI-based implementations for neural network processing elements and convolution operations.	Apply
CO4	Utilize the architectural principles of standard CNN models such as LeNet, AlexNet, and ResNet.	Apply
CO5	Apply VLSI architectures for deep neural networks, focusing on processing optimization and hardware acceleration techniques.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	10	-	-	30	-
Understand	30	10	30	10	10	60	10
Apply	10	90	20	90	90	10	90
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology - Autonomous R 2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 504 - Machine Learning in VLSI System Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	2	0	2	60	3	50	50	100

Introduction to Machine Learning Architecture* Artificial Neural Networks – Artificial Neuron and its mathematical model - Neural network architecture: single layer and multilayer feed forward networks, Learning Paradigms- Supervised, Unsupervised and reinforcement Learning, Architecture for Multiply and Accumulate unit.	[6]
Supervised Learning and Unsupervised Learning* Multilayer Perceptron - Back propagation learning algorithm, Radial-basis function Networks Kernels and Support vector machines, Unsupervised learning - K means	[6]
VLSI Implementation of Neural Networks* Processing element model, PE row, PE array design - Processing element tile design - Direct, FFT-based, Winograd-based, Matrix multiplication based convolutional strategies	[6]
Deep Neural Networks* Convolutional Neural basics: kernels, padding, stride, channels, and activation maps - Standard CNN architectures: AlexNet, ResNet.	[6]
VLSI Architecture for Deep Neural Networks* VLSI architecture for deep neutral networks, data and instruction flow in 2D systolic array architecture - Processing optimization in 2D systolic array - Hardware Accelerator.	[6]
Practical: 1. Simulate the data extraction from the database and various data pre-processing techniques for a given dataset. 2. Simulate the ANN using back-propagation algorithm. 3. Simulate a regression model for a given dataset. 4. Simulate SVM classification for a dataset. 5. Simulate a decision tree classification model for a given dataset. 6. Simulate dimensionality reduction using PCA method on a given dataset. 7. Simulate dimensionality reduction using ICA method on a given dataset. 8. Simulate K mean clustering method. 9. Simulate and optimize data flow and processing in a 2D systolic array. 10. Simulate a PE row and array for neural network computations.	[30]
Total Hours:	60

Text Book(s):	
1.	Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag.
2.	Ethem Alpaydin, Introduction to Machine Learning, PHI
Reference(s):	
1.	Jose G. Delgado-Frias, William R. Moore, “VLSI For Artificial Intelligence And Neural Networks”, Springer Science Business Media, LLC, 2001.
2.	Mohamed I. Elmasry, “VLSI Artificial Neural Networks Engineering”, Springer Science Business Media, LLC, 2000.
3.	Sied Mehdi Fakhraie, Kenneth C. Smith, “VLSI - Compatible Implementations for Artificial Neural Networks”, Springer Science Business Media, LLC, 1996
4.	Gray and Meyer, ‘‘Analysis and Design of Analog Integrated Circuits’‘, 5th Edition, Wiley International, 2010.

*SDG 9 - Sustainable industrialization and foster innovation

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Introduction to Machine Learning Architecture**	
1.1	Artificial Neural Networks.	1
1.2	Artificial Neuron and its mathematical model	1
1.3	Neural network architecture: single layer	1
1.4	Multilayer feed forward networks, Learning Paradigms-Supervised,	1
1.5	Unsupervised, Reinforcement Learning	1
1.6	Architecture for Accumulate unit, Architecture for Multiply unit	1
2	**Supervised Learning and Unsupervised Learning***	
2.1	Multilayer Perceptron	1
2.2	Back propagation learning algorithm	1
2.3	Radial-basis function Networks Kernels	1
2.4	Support vector machines	1
2.5	Unsupervised learning	1
2.6	K Means	1
3	**VLSI Implementation of Neural Networks***	
3.1	Processing element model	1
3.2	PE row	1
3.3	PE array design	1
3.4	Processing element tile design	1
3.5	Direct, FFT-based, Winograd-based	1
3.6	Matrix multiplication based convolutional strategies	1
4	**Deep Neural Networks***	
4.1	Convolutional Neural basics: kernels,	1
4.2	Padding, stride,	1
4.3	channels, activation maps	1
4.4	Standard CNN architectures: AlexNet, ResNet	1
5	**VLSI Architecture for Deep Neural Networks***	
5.1	VLSI architecture for deep neutral networks,	2
5.2	data and instruction flow in 2D systolic array architecture -	1
5.3	Processing optimization in 2D systolic array	1
5.4	Hardware Accelerator.	2
Practical:		
1.	Simulate the data extraction from the database and various data pre-processing techniques for a given dataset.	2
2.	Simulate the ANN using back-propagation algorithm.	2
3.	Simulate a regression model for a given dataset.	2
4.	Simulate SVM classification for a dataset.	2
5.	Simulate a decision tree classification model for a given dataset.	2
6.	Simulate dimensionality reduction using PCA method on a given dataset.	4
7.	Simulate dimensionality reduction using ICA method on a given dataset.	4
8.	Simulate K mean clustering method.	4
9.	Simulate and optimize data flow and processing in a 2D systolic array.	4
10.	Simulate a PE row and array for neural network computations.	4

Course Designer(s)

1. Mr.D.Poornakumar-Poornakumard@ksrct.ac.in

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60 MY 003	Startups and Entrepreneurship	Category	L	T	P	Credit
		MY	2	0	0	2##

Objectives

- To Learn basic concepts in entrepreneurship, develop mind-set and skills necessary to explore entrepreneurship
- To provide practical proven tools for transforming an idea into a product or service that creates value for others.
- To Comprehend the process of opportunity identification through design thinking, identify market potential and customers while developing a compelling value proposition solution and prototypes
- To create business plan, conduct financial analysis and feasibility analysis to assess the financial viability of a venture ideas & solutions built with domain expertise
- To Prepare and present an investible pitch deck of their practice venture to attract stakeholders

Pre-requisites

- Basic knowledge of reading and writing in English

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop an entrepreneurial mindset and appreciate the concepts of design thinking, entrepreneurship and innovation	Understand
CO2	Apply process of problem -opportunity identification and validation through human centred approach to design thinking in building solutions	Apply
CO3	Understand market types, conduct market estimation, identify customers, create customer persona, develop the skills to create a compelling value proposition and build a Minimum Viable Product	Apply
CO4	Create business plan, conduct financial analysis and feasibility analysis to assess the financial viability of a venture	Apply
CO5	Prepare and deliver an investible pitch deck of their practice venture to attract stakeholders	Create

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	1	3	1	2	1	-	2	2	3	3	-
CO2	2	3	3	2	2	-	2	2	2	-	2	2	2	3	-
CO3	3	2	3	1	2	-	-	-	1	3	1	3	3	2	-
CO4	3	3	3	3	3	2	2	1	-	1	3	3	3	3	-
CO5	3	2	3	3	3	-	-	2	-	-	3	2	3	2	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		Pitch Deck final submission & Via voce
	Milestone 1 (25 Marks)	Milestone 1 (25 Marks)	
Remember	10	-	50
Understand	05	10	
Apply	10	10	
Analyse	-	-	
Evaluate	-	5	
Create	-	-	
Total	25	25	

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design & Technology)

60 MY 003 - Startups and Entrepreneurship

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	2	0	0	30	2##	100	-	100

Introduction to Entrepreneurship & Entrepreneur Meaning and concept of Entrepreneurship, the history of Entrepreneurship development, Myths of Entrepreneurship, role of Entrepreneurship in Economic Development, Agencies in Entrepreneurship Management and Future of Entrepreneurship. The Entrepreneur: Meaning, the skills required to be an entrepreneur, the entrepreneurial decision process, Role models, Mentors and Support system, Innovation and Creativity, types of innovations, Innovations in current scenario	[6]
Problem-Opportunity Identification, Customers Discovery and competitive advantage Understanding the Problem and opportunity, define problem using Design thinking principles and validate problem. Exploring market types and estimating the market size, knowing your customer and consumer, Customer segmentation and creating customer personas. Importance of Value Proposition, Value Proposition Canvas, Developing Problem-solution fit, Competition analysis, Blue ocean strategy, Competitive positioning and understanding unique selling points.	[6]
Business model and build your MVP Introduction to Business model and types, Lean approach, 9 block lean canvas model, riskiest assumptions to Business models. Prototyping, building a Minimum viable product, Hypothesis testing and MVP Validation, MVP Iteration-Importance of Build - Measure – Learn approach	[6]
Business Plan, Financial feasibility and Managing growth Business planning: components of Business plan- Sales plan, People plan and financial plan, Preparing a business plan. Financial Planning: Types of costs, preparing the financial plan using financial template, understanding basics of Unit economics and analyzing Growth and the financial performance	[6]
Go To Market Strategies and Funding Introduction to Go to market strategies, start-up branding and its elements, Selecting the Right Channel, creating digital presence, building customer acquisition strategy. Choosing a form of business organization specific to your venture, identifying sources of funds: Debt & Equity, Map the Start-up Lifecycle to Funding Options, Build an Investor ready pitch deck.	[6]
Total Hours:	**30**

Text Book(s):

1.	Stephen Key, “One Simple Idea for Startups and Entrepreneurs: Live Your Dreams and Create Your Own Profitable Company” 1st Edition, Tata Mc Grawhill Company, New Delhi, 2013.
2.	Charles Bamford and Garry Bruton, “Entrepreneurship: The Art, Science, and Process for Success”, 2nd Edition, Tata Mc Grawhill Company, New Delhi, 2016.

Reference(s):

1.	Philip Auerswald, “The Coming Prosperity: How Entrepreneurs Are Transforming the Global Economy”, Oxford University Press, 2012.
2.	Janet Kiholm Smith; Richard L. Smith Richard T. Bliss, “Entrepreneurial Finance: Strategy, Valuation and Deal Structure, Stanford Economics and Finance”, 2011.
3.	Edward D. Hess, “Growing an Entrepreneurial Business: Concepts and Cases”, Stanford Business Books, 2011.
4.	Ignite program, wadhwani platform, Entrepreneurship, NPTEL online course By Prof. C Bhaktavatsala Rao | IIT Madras

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Introduction to Entrepreneurship & Entrepreneur**	
1.1	Meaning and concept of Entrepreneurship and the history of Entrepreneurship development	1
1.2	The Entrepreneur: Meaning, the skills required to be an entrepreneur, the entrepreneurial decision process,	1
1.3	Myths of Entrepreneurship, How to Become a Successful Entrepreneur - Dr Romesh Wadhwani (Platform on boarding)	1
1.4	Role models, Mentors and Support system- Masterclass on My Story - Joshua Salins	1
1.5	Role of Entrepreneurship in Economic Development, Agencies in Entrepreneurship Management and Future of Entrepreneurship	1
1.6	Innovation and Creativity, types of innovations, Innovations in current scenario, Concepts of Entrepreneurial Thinking, General Enterprising tendency test	1
2.0	**Problem-Opportunity Identification, Customers Discovery and competitive advantage**	
2.1	Understanding the Problem and opportunity, define problem using Design thinking principles and validate problem. Case study and Fireside chat – Desi Hangover	1
2.2	Identifying a problem for practice venture and filling Problem statement canvas (Handout week 1 - class activity)	1
2.3	Customer and markets discovery , knowing your customer and consumer, Customer segmentation and Exploring market types and estimating the market size. Case study and Fireside chat – Verloop	1
2.4	Creating customer personas & Market estimation (Handout week 2 - class activity)	1
2.5	Importance of Value Proposition, Introduce Value Proposition Canvas, Developing Problem-solution fit. Case study and Fireside chat – Honey Twigs	1
2.6	Competition analysis, Blue ocean strategy, Competitive positioning and understanding unique selling points. Case study and Fireside chat on Inzpira Fill Value Proposition Canvas (Handout week 3 - class activity) and Competition analysis framework (Handout week 5 - class activity) **Briefing on Assignment 1 - Milestone 1**	1
3.0	**Business model and Build your MVP**	
3.1	Introduction to Business model and types. Case study and Fireside chat – NUOS	1
3.2	Lean approach, 9 block lean canvas model, riskiest assumptions to Business models	1
3.3	Class Activity- Fill Lean canvas for you idea and understand revenue model (Handout week 6)	1
3.4	Prototyping, Meaning of MLP , Difference between MLP and MVP, How to build an MLP? Different types MLP that you can build. Case study and Fireside chat – KNORISH	1
3.5	Hypothesis testing and MVP Validation, MVP Iteration-Importance of Build - Measure – Learn approach	1
3.6	Class Activity- Fill MVP framework (Handout week 7) and learn validation	1
4.0	**Business Plan, Financial feasibility and Managing growth**	
4.1	Business planning: components of Business plan- Sales plan, People plan and financial plan, Preparing a business plan. Case study and Fireside chat – Bodh Gems	1
4.2	Financial Planning: Types of costs, preparing the financial plan using financial template (Handout week 9)	1
4.3	Class activity - starting up costs, COGS, Sales plan and people plan template.	1
4.4	Class activity - One year P&L projection, Breakeven Analysis, Five year projection	1
4.5	Understanding basics of Unit economics and analyzing Growth and the financial performance	1
4.6	Class activity - Financial template - Unit economics (Handout week 12)	1

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5.0	**Go to Market Strategies and Funding**	
5.1	Introduction to Go to market strategies, start-up branding and its elements, Selecting the Right Channel	1
5.2	Creating digital presence, building customer acquisition strategy.	1
5.3	Class activity: Handout week 10 - create your GTM strategy	1
5.4	Choosing a form of business organization specific to your venture	1
5.5	Identifying sources of funds: Debt & Equity, Map the Start-up Lifecycle to Funding Options	1
5.6	Class activity - Visit relevant GOI websites, other sites to help students explore funding opportunities and briefing on final submission of the pitch deck Build an Investor ready pitch deck, What Should You Cover in Your Pitch Deck? Art of pitching and storytelling	1

Course Designer(s)

1. Dr.N.Tiruvenkadam - tiruvenkadam@ksrct.ac.in

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60 EV 5P1	VLSI Laboratory	Category	L	T	P	Credit
		PC	0	0	3	1.5

Objectives

- To learn hardware descriptive language
- To learn the fundamental principles of digital system design using HDL and FPGA
- To learn the fundamental principles of VLSI circuit design in digital domain
- To learn the fundamental principles of VLSI circuit design in analog domain
- To provide hands on design experience with EDA platforms

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop HDL code for basic as well as advanced digital circuit	Apply
CO2	Implement various logic modules into FPGA	Apply
CO3	Synthesize place and route the digital IPs	Apply
CO4	Design, simulate and extract the layouts of digital circuits using EDA tools	Apply
CO5	Design various arithmetic building blocks using HDL	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	25	12	50	50
Apply	25	13	50	50
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 5P1 - VLSI Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	0	0	3	45	1.5	60	40	100

List of Experiments*:

1. Design and verify basic combinational circuits (Full Adder and Multiplexer) with test bench code. Simulate it using the EDA tool and implement it using an FPGA.
2. Design and verify basic sequential circuits (Universal Shift Register and Synchronous Counter) with test bench code. Simulate it using the EDA tool and implement it by FPGA.
3. Design 4-bit ALU with test bench code. Simulate it using the EDA tool and implement it by FPGA.
4. Design Finite State Machine (Moore/Mealy) using HDL. Simulate it using the EDA tool.
5. Design and simulate a CMOS NAND. Generate Layout.
6. Design and simulate a D-Flip-Flop. Generate Layout.
7. Design and simulate an inverting amplifier. Generate Layout.
8. Design memories using HDL. Simulate it using EDA tool*.
9. Design carry save adder using arithmetic building blocks using HDL
10. Design Booth multiplier using arithmetic building blocks using HDL.

Lab Manual

1.	"VLSI Laboratory Manual", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 9 - Industry Innovation and Infrastructure

Course Designer(s)

1. Mrs.C.Saranya - saranyac@ksrct.ac.in

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(VLSI Design and Technology)
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Tiruchengode - 637 215

60 EV 5P2	Signal Processing Laboratory	Category	L	T	P	Credit
		PC	0	0	3	1.5

Objectives

- To implement FIR and IIR filters using simulation.
- To design a DSP system to demonstrate the multi-rate signal processing concepts.
- To analyse the effects of sampling and quantization errors in signals.
- To simulate waveforms and process of mathematical operations of Digital Signal Processing.
  To design and implement digital filters and adaptive filters for given specifications and applications in DSP system.

Pre-requisites

- Signals and Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design of IIR and FIR filters and verify its performance using simulation	Apply
CO2	Design of multirate filters and verify its performance using simulation	Apply
CO3	Evaluate the effects of quantization errors in continuous time signals	Apply
CO4	Generate standard waveform and compute arithmetic operation using Digital Signal Processor	Apply
CO5	Design of IIR, FIR, multirate and adaptive filters and verify its performance using Digital Signal Processor	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	3	3	3	-	3	3	3	2
CO2	3	3	3	-	3	-	-	3	3	3	-	3	3	3	2
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	2
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	2
CO5	3	3	3	-	3	-	-	3	3	3	-	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	20	10	30	30
Apply	30	15	70	70
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 5P2 - Signal Processing Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	0	0	3	45	1.5	60	40	100

List of Experiments*:

Using Simulation

1. Design of IIR filters
2. Design of FIR filters
3. Design of Multirate filters
4. Analyse the effect of quantization on continuous time analog signals

Using DSP Processor

5. Generation of standard waveforms
6. Implementation of arithmetic operations
7. Design and implementation of FIR & IIR filter for real time applications
8. Implementation of adaptive filter

- Mini Project

Lab Manual

1.	"Digital Signal Processing Laboratory", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG:4 - Quality Education

Course Designer(s)

1. Mr.S.Pradeep-pradeeps@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 5P3	Design Thinking and Innovation Laboratory	Category	L	T	P	Credit
		PC	0	0	2	1

Objectives

- Understand the principles of design thinking and their application in engineering innovation
- Identify real-world engineering problems through brainstorming and mind mapping
- Explore problem space using secondary research methods, including the 5Ws and 1H Matrix, and user participant mapping
- Conduct primary research from multiple perspectives to ensure a user-centered approach
- Define and analyze problem areas to develop clear and well-structured problem statements

Pre-requisites

-Nil-

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply design thinking principles to promote innovation.	Apply
CO2	Identify and articulate real-world engineering problems through brainstorming and mind map techniques.	Apply
CO3	Perform secondary research using tools 5Ws and 1H Matrix and user participant mapping to explore problem spaces.	Apply
CO4	Conduct primary research to gather insights from diverse perspectives, ensuring a user- centered approach in problem-solving.	Apply
CO5	Define and analyze problem areas to create precise and actionable problem statements.	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	-	-	-	3	3	3	-	-	3	3	3
CO2	3	-	-	-	-	3	3	3	3	3	-	-	3	3	3
CO3	3	-	-	-	-	-	-	3	3	3	-	-	3	3	3
CO4	3	-	-	-	-	-	-	3	3	3	-	-	3	3	3
CO5	3	3	-	-	-	-	-	3	3	3	-	-	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Review I (CO1)			Review II (CO2,CO3,CO4)			Review III (CO5)			Total (R1+R2+R3)	Internal
Identification of Existing Problems and Solutions	Apply design thinking principles	Case study report	Selection of Problem	Secondary and Primary Research on Problem Space	Presentation	Analysis of Problem Space	OIOR	Presentation	Total	
10	10	10	10	30	10	5	10	5	100	60

Report and Presentation (CO1, CO2, CO3, CO4 & CO5)			External
Report	Presentation	Total	
50	50	100	40

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E – Electronics Engineering (VLSI Design & Technology)								
60 EV 5P3 – Design Thinking and Innovation Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	0	0	2	30	1	60	40	100

Design Thinking and Innovation Process Introduction to Design Thinking and Innovation - Design, Design Thinking, Innovation - Stages of Design Thinking Process – Case Study: Analysis of Existing Problems and Solutions.	[8]
Selection of Problem Identification and Selection of Problem to Solve, Tools - Brain-storming- Sorting & affinity-Links, Mind-mapping- affinity-Links.	[4]
Secondary research on Problem Space Information Gathering: from past and existing - Secondary Research - Ask questions: Why, who, what, where, when, how, etc, 5Ws and 1H Matrix Table - User Participant Mapping.	[6]
Primary research on Problem Space Understanding your Users environment - Primary research - Observation, Conversations, Questionnaires, Documentation - Conducting Contextual Inquiry.	[6]
Analysis of Problem Space Identify, Classify, Compare, Prioritize, Cross-relate information - Personas Observations, Inference, Opportunities, Recommendations (OIOR) - Redefining the Problem Statement.	[6]
Total Hours:	30

Reference

1.	• NPTEL: Design Thinking and Innovation by Prof. Ravi Poovaiah, IDC School of Design, IIT Bombay. https://onlinecourses.swayam2.ac.in/aic23_ge17/preview, https://dsource.in/dti • NPTEL: Design, Technology and Innovation by Prof. B. K. Chakravarthy, IDC School of Design, IIT Bombay. https://onlinecourses.nptel.ac.in/noc20_de03/preview • NPTEL: Innovation by Design by Prof. B. K. Chakravarthy, IDC School of Design, IIT Bombay, https://onlinecourses.swayam2.ac.in/aic19_de02/preview., • www.dsource.in , The Resource for Design by e-Kalpa Design Team, IDC, IIT Bombay,DoD, IIT Guwahati & NID, Bengaluru.

*SDG 9 – Industry Innovation and Infrastructure

Course Designer(s)

1. Dr.K.Raja – raja@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 CG 0P4	Career Skill Development - IV	Category	L	T	P	Credit
		CG	0	0	2	1*

Objectives

- To help learners improve their vocabulary and enable them to use words appropriately in different academic and professional contexts.
- To help learners develop strategies that could be adopted while reading texts.
- To help learners acquire the ability to speak and write effectively in english in real life and career related situations.
- Improve listening, observational skills, and problem-solving capabilities
- Develop message generating and delivery skills

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Compare and contrast products and ideas in technical texts.	Analyse
CO2	Identify cause and effects in events, industrial processes through technical texts	Analyse
CO3	Analyse problems in order to arrive at feasible solutions and communicate them orally and in the written format.	Analyse
CO4	Report events and the processes of technical and industrial nature.	Apply
CO5	Articulate their opinions in a planned and logical manner, and draft effective résumés in context of job search.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2	2	2	3	-	3	-	-	-	2	3	3	3	2	2
CO2	3	3	3	3	-	2	-	-	-	2	3	3	3	2	2
CO3	2	2	2	2	-	3	-	-	-	2	3	3	3	2	2
CO4	3	3	3	3	-	2	-	-	-	2	3	3	3	2	2
CO5	3	3	3	3	-	2	-	-	-	2	3	3	3	2	2

3 - Strong; 2 - Medium; 1 - Some

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design & Technology)

60 CG 0P4 - Career Skill Development - IV

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	0	0	2	30	1*	100	-	100

Verbal & Analytical Reasoning* Seating Arrangements - Analytical Reasoning (PUZZELS) - Machin Input And Output - Coded Inequality - Eligibility Test.	[6]
Quantitative Aptitude - Part - 4* Permutation and Combination - Probability - Quadratic Equation - Geometry - Clock - Calendar - Logarithmic.	[6]
Non-Verbal Reasoning * Series Completion of Figures - Classification - Courting of figure - Figure matrix - Embedded Figure - Complete Figure - Paper Cutting and Folding - Mirror images and Water Images.	[6]
Quantitative Aptitude - Part - 5* Mensuration of Area, Volume and Surface area in 2D and 3D Shapes - 2D Shapes - Square, Rectangle, Triangle, Circle, etc. - 3D Shapes - Cube, Cuboid , Sphere , Cone , etc.	[6]
Data Interpretation and Analysis* Data interpretation Based on text - Data interpretation Based on Tabulation, Pie chart, Bar graph and Line graph - Venn Diagram - Data sufficiency.	[6]
Total Hours:	**30**

Reference(s):

1.	Aggarwal, R.S. “A Modern Approach to Verbal and Non-verbal Reasoning”, Revised Edition 2008, S.Chand & Co Ltd., New Delhi, Reprint 2009
2.	Abhijit Guha, “Quantitative Aptitude”, McGraw Hill Education, 6th edition, 2016.
3.	Dinesh Khattar, “Quantitative Aptitude For Competitive Examinations”, Pearson Education - 2020
4.	Anne Thomson, “Critical Reasoning: A Practical Introduction” Lexicon Books, 3rd edition, 2022.

*SDG 4 - Quality Education
*SDG 8 - Decent work and Economic growth
*SDG 9 - Industry, innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Verbal & Analytical Reasoning**	
1.1	Seating Arrangements	1
1.2	Analytical Reasoning (Puzzels)	1
1.3	Machin Input And Output	1
1.4	Coded Inequality	1
1.5	Eligibility Test	2
2.0	**Quantitative Aptitude - Part - 4**	
2.1	Permutation And Combination	1
2.2	Probability	1
2.3	Quadratic Equation - Geometry	1
2.4	Clock - Calendar	1
2.5	Logarithmic	2
3.0	**Non-Verbal Reasoning**	
3.1	Series Completion of Figures - Classification	1
3.2	Courting of Figure - Figure Matrix	1
3.3	Embedded Figure - Complete Figure	1
3.4	Paper Cutting and Folding	1
3.5	Mirror Images and Water Images	2
4.0	**Quantitative Aptitude - Part - 5**	
4.1	Mensuration of Area, Volume	1
4.2	Mensuration of Volume	1
4.3	Surface Area In 2D And 3D Shapes	1
4.4	2D Shapes - Square, Rectangle, Triangle, Circle, Etc.	1
4.5	3D Shapes - Cube, Cuboid , Sphere , Cone , Etc.	2
5.0	**Data Interpretation and Analysis**	
5.1	Data Interpretation Based on Text	1
5.2	Data Interpretation Based on Tabulation, Pie Chart	1
5.3	Bar Graph and Line Graph	1
5.4	Venn Diagram	1
5.5	Data Sufficiency	2
	Total	**30**

Course Designer(s)

1. R. Poovarasan - poovarasan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS

(For the candidates admitted in 2025-2026)

SIXTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EV 601	Embedded Systems	2	40	60	100	45	100
2.	60 EV 602	Testing of VLSI Circuits	2	40	60	100	45	100
3.	60 EV 604	Analog and Digital Communication	2	40	60	100	45	100
4.	60 EV E2*	Professional Elective II	2	40	60	100	45	100
5.	60 OE L3*	Open Elective III	2	50	50	100	45	100
6.	60 MY 004	Disaster Management	2	100	00	100	00	100
THEORY CUM PRACTICAL								
7.	60 EV 603	ASIC Design	2	50	50	100	45	100
PRACTICAL								
8.	60 EV 6P1	VLSI Verification and Testing Laboratory	3	60	40	100	45	100
9.	60 EV 6P2	Embedded Systems Laboratory	3	60	40	100	45	100
10.	60 EV 6P3	Design Thinking and Product Development Laboratory	3	60	40	100	45	100
11.	60 CG 0P5	Comprehension Test	1	100	-	100	-	100
12.	60 CG 0P6	Internship	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination, 50 marks for theory cum practical End Semester Examination and 40 marks for practical End Semester Examination.

Passed in BoS Meeting held on 20/12/2025
Approved in Academic Council Meeting held on 03/01/2026

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 601	Embedded Systems	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To impart the knowledge of the Embedded design
- To learn the architecture and features of ARM Cortex
- To learn the functionality and its features of ARM Cortex Peripherals
- To program the CORTEX M3
- To impart the working of Embedded operating system

Pre-requisites

- Microprocessors and Microcontrollers, Basics of C Programming

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the overall landscape and characteristics of embedded systems	Understand
CO2	Discuss the architecture and features of ARM CORTEX	Understand
CO3	Analyse the functionalities of ARM CORTEX-M3/M4 peripherals and develop programs	Apply
CO4	Develop programs to access the features of ARM CORTEX M3/M4	Apply
CO5	Discuss the architecture of the real time operating system and its operations	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	-	-	-	-	3	3	3	-	3	3	2	3
CO2	3	3	3	-	3	-	-	3	3	3	-	3	3	2	3
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	2	3
CO4	3	3	3	3	3	-	-	3	3	3	-	3	3	2	3
CO5	3	3	3	-	3	-	-	3	3	3	-	3	3	2	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	20
Understand	40	20	20
Apply		30	60
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology - Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 601 - Embedded Systems								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Embedded Computing* Characteristics of Embedded Computing -Challenges In Embedded Computing System Design - Embedded System Design Process - Embedded Hardware Units and Devices In a System - Embedded Software In a System - Examples of Embedded System - Classifications of Embedded System-Skills Required for an Embedded System Designer.	[9]
Embedded Networks* Embedded Networks - Distributed Embedded Architectures - Network Protocols: RS485, CAN, USB, Wireless: Wi-Fi and Lora. Case Study: Automatic Chocolate Vending Machine and Digital Camera, Elevator Controller.	[9]
ARM Architecture* Advanced RISC Machine -Architecture Inheritance, ARM Programming Model - 3 And 5 Stages Pipeline ARM Organization, ARM Instruction Execution and Implementation - Thumb Bit In The CPSR - Thumb Programmer's Model, Architectural Support for System Development - Memory Interface, JTAG IEEE1149.	[9]
LPC 214x Microcontroller* Key Features, Architectural, Block Diagram, Pinning Information, Memory Map, Interrupt Controller, Interrupt Sources, System Control Block Functions, Application Information, ARM Development Tool, ARM Programming.	[9]
Real Time Operating Systems* Principles of OS - OS Architecture - System Calls - Threads, Tasks And Process - Task States - Kernel and Its Function - Scheduling: Static, Dynamic, Priority, Pre-Emptive, Round Robin, Earliest Deadline First, Rate Monotony, First-Come, First-Served (FCFS). Shortest-Job-Next, Multiple - Level Queues Scheduling.	[9]
Total Hours:	**45**

Text Book(s):	
1.	Rajkamal, "Embedded Systems Architecture: Programming and Design", 2nd Edition, Tata McGraw Hill, 2014.
2.	Steve Furber, "ARM System on chip Architecture", 2nd Edition, Addison Wesley, 2017.
Reference(s):	
1.	Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", 2nd Edition, Morgan Kaufman Publishers, 2013.
2.	David E.Simon, "An Embedded Software Primer", 3rd Edition, Pearson Education, 2014.
3.	Dr.Prasad K.V.K.K, "Embedded/Real-Time systems: Concepts, Design& Programming", New Edition, Dream Tech Press, 2013.
4.	Joseph Yiu, "The Definitive Guide to the ARM Cortex-M", Elsevier- Newness, 2014.

* SDG: 9 - Industry, Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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Tiruchengode - 637 215

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Structure of Embedded Systems**	
1.1	Embedded Computing: Characteristics of Embedding Computing Applications	1
1.2	Embedded System Architecture: Instruction Set Architecture, CISC and RISC	1
1.3	Embedded C Data types and variables	1
1.4	Storage classes	1
1.5	Register data assignment	1
1.6	Bitwise operation – AND, OR, NOT	1
1.7	Bitwise operation – Bit shifting	1
1.8	GPIO: Overview,	1
1.9	Interfacing	1
2.0	**ARM CORTEX-M3 Architecture**	
2.1	ARM Architecture – Versions	1
2.2	CORTEX-M3/M4 Microcontroller: Block diagram	1
2.3	Bus architecture	1
2.4	Reset value of a register, Register bit positions	1
2.5	UART: Protocol – Data frame	1
2.6	UART: Protocol – Handshaking	1
2.7	Port accessing – GPIO as Input / output	1
2.8	Port accessing – BSRR	1
2.9	Error management	1
3.0	**Peripherals in CORTEX M3**	
3.1	Operation Mode, Exceptions and Interrupts	1
3.2	Vector Tables	1
3.3	Stack Memory Operations	1
3.4	Reset Sequence	1
3.5	CORTEX M3 Instruction Sets: Assembly Basics	1
3.6	SAR ADC, HAL_ADC module	1
3.7	Conversion modes, Resolution	1
3.8	HAL_DAC module, Pin assignments	1
3.9	I2C Interfacing	1
4.0	**CORTEX M3 Programming**	
4.1	Development Flow, Volatile and effect of optimization	1
4.2	Interrupt handling	1
4.3	Timer Interrupt	1
4.4	SysTick Timer	1
4.5	Watchdog Timer	1
4.6	SPI Peripherals	1
4.7	SPI testing	1
4.8	EEPROM Interface – Write Data	1
4.9	EEPROM Interface – Read Data	1
5.0	**Real Time Operating Systems**	
5.1	OS: Basic principles, Architecture	1
5.2	System calls	1
5.3	Threads, tasks and process	1
5.4	Kernel and its function	1
5.5	Scheduling: static, dynamic, priority	1
5.6	Interrupt APIs	1
5.7	Task Creation API	1
5.8	Low Power Management with RTOS	1
5.9	RTOS vs Embedded Linux	1

Course Designer(s)

1.Mr.T.Rajavenkatesan-rajavenkatesan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 602	Testing of VLSI Circuits	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To know the various types of faults in digital circuits
- To learn the concepts of fault modelling
- To acquire knowledge in test vectors generation for combinational and sequential circuits
- To know the test generation concepts in dft, bist
- To study the concepts in fault diagnosis

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Examine the various concepts of testing and methods of fault model in VLSI circuits.	Analyse
CO2	Analyse test generation of various algorithms for digital circuits.	Analyse
CO3	Describe the various techniques for testability	Understand
CO4	Discuss the various types of architecture and test algorithm for BIST.	Understand
CO5	Design the self - checking circuit for fault diagnosis of VLSI circuits.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	-	10	-
Understand	30	50	70
Apply	10	-	10
Analyse	20	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 602 - Testing of VLSI Circuits								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Testing and Fault Modelling* Faults In Digital Circuits – Modelling of Faults – Logical Fault Models – Fault Detection – Fault Location – Fault Dominance – Logic Simulation – Types of Simulation – Delay Models.	[9]
Test Generation* Test Generation for Combinational Logic Circuits – Testable Combinational Logic Circuit Design – Test Generation for Sequential Circuits.	[9]
Design for Testability* Design for Testability – Ad-Hoc Design – Generic Scan Based Design - System Level DFT Approaches.	[9]
Memory and Delay Fault Testing* Built-In Self Test – Test Pattern Generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms. Testable Memory Design - RAM Fault Models - Test Algorithms For Rams - Delay Faults-Delay Test.	[9]
Fault Diagnosis* Logical Level Diagnosis – Diagnosis by UUT Reduction – Fault Diagnosis for Combinational Circuits – Self-Checking Design.	[9]
Total Hours:	**45**

Text Book(s):	
1.	Abramovici M.,.Breuer M.A and Friedman A.D., “Digital systems Testing and Testable Design”, Jaico Publishing House, 2013.
2.	Lala P.K., “Digital Circuit Testing and Testability”, Academic Press, 2012.
Reference(s):	
1.	Bushnell M.L. and Agrawal V.D, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Springer US, 2013.
2.	Crouch A.L., “Design-For-Test For Digital IC’s and Embedded Core Systems”, Pearson Education, 2012.
3.	Jha N. & Gupta S.D., “Testing of Digital Systems”, Cambridge, 2003.
4.	Wen W. W., “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers, 2006.

*SDG:4- Quality Education

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Testing and Fault Modelling**	
1.1	Testing of VLSI	1
1.2	Faults In Digital Circuits	1
1.3	Modelling of Faults	1
1.4	Logical Fault Models	1
1.5	Fault Detection, Fault Location	1
1.6	Fault Dominance	1
1.7	Logic Simulation	1
1.8	Types of Simulation	1
1.9	Delay Models	1
2.0	**Test Generation**	
2.1	Test Generation for Combinational Logic	3
2.2	Testable Combinational Logic Circuit Design	3
2.3	Test Generation for Sequential Circuits	3
3.0	**Design for Testability**	
3.1	Design for Testability	3
3.2	Ad-Hoc Design	2
3.3	Generic Scan Based Design	2
3.4	System Level DFT Approaches	2
4.0	**Memory and Delay Fault Testing**	
4.1	Built-In Self Test	1
4.2	Test Pattern Generation for BIST	1
4.3	Circular BIST	1
4.4	BIST Architectures	1
4.5	Testable Memory Design	1
4.6	Test Algorithms	1
4.7	Testable Memory Design	1
4.8	RAM Fault Models	1
4.9	Test Algorithms for Rams- Delay Faults-Delay Test	1
5.0	**Fault Diagnosis**	
5.1	Logical Level Diagnosis	2
5.2	Diagnosis by UUT reduction	2
5.3	Fault Diagnosis for Combinational Circuits	3
5.4	Self-Checking Design	2

Course Designer(s)

1. Mr S.Pradeep – pradeeps@ksrct.ac.in

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60 EV 603	ASIC Design	Category	L	T	P	Credit
		PC	3	0	2	4

Objectives

- To understand the fundamental steps of the Physical Design flow, focusing on strategic floorplanning, power grid distribution, and I/O cell placement.
- To explore various placement algorithms and optimization techniques like Simulated Annealing to ensure minimal area and timing-driven cell positioning.
- To master the principles of Global and Detailed routing, including interconnect delay measurement and the application of the Left-Edge algorithm for area efficiency.
- To analyze timing parameters and constraints, specifically focusing on setup and hold checks, clock skew, and the identification of false or multicycle paths.
- To perform signoff verification procedures, covering DRC, LVS, and Signal Integrity analysis to ensure the manufacturability and reliability of the final layout.

Pre-requisites

- VLSI and Chip Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the fundamental stages of the physical design cycle and the specific objectives of floorplanning, power planning, and clock planning.	Understand
CO2	Apply iterative placement algorithms and simulated annealing techniques to determine the optimal spatial positioning of logic cells in a design.	Apply
CO3	Apply the Left-Edge algorithm and area-routing methods to successfully define channels and establish interconnects between functional blocks.	Apply
CO4	Understand the definitions of setup and hold timing and the impact of clock skew, jitter, and false paths on overall circuit performance.	Understand
CO5	Understand the critical signoff checks, including DRC and LVS, and the importance of crosstalk analysis in ensuring design reliability and yield.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	2	-	-	-	-	-	-	-	2	2	-
CO2	3	3	-	-	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	-	-	3	-	-	-	-	-	-	-	3	3	-
CO4	3	3	-	-	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	2	2	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	20	-	-	20	-
Understand	60	-	50	-	-	60	-
Apply	20	50	30	50	50	20	50
Analyse	-	50	-	50	50	-	50
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 603 - ASIC Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	2	75	4	50	50	100

Floor Planning* Overview of Physical Design flow, Floorplanning Goals and Objectives, Measurement of Delay in Floorplanning, Floorplanning Tools, Channel Definition, I/O and Power Planning, Clock Planning.	[9]
Placement* Placement Goals and Objectives, Placement Algorithms, Eigenvalue Placement, Iterative Placement Improvement, Placement Using Simulated Annealing, Timing-driven floorplanning and placement design flow, Information Formats.	[9]
Routing* Global Routing: Goals and Objectives, Measurement of Interconnect Delay, Global Routing Methods, Global Routing Between Blocks, Global Routing Inside Flexible Blocks, Timing-Driven Methods, Back-annotation, Detailed Routing: Goals and Objectives, Measurement of Channel Density, Algorithms-Left-Edge Algorithm, Constraints and Routing Graphs, Area-Routing Algorithms, Multilevel Routing, Timing-Driven Detailed Routing.	[9]
Timing Analysis* Timing Parameter Definition - Setup Timing Check- Hold Timing Check- Multicycle PathsHalf-Cycle Paths- False Paths- Clock skew- Setup and Hold Violation Fixin- Origins of Clock Skew/Jitter and impact on Performance.	[9]
Signoff Checks* Physical Design Verification: Signoff DRC- LVS Timing Signoff: DRV Checks-Setup-HoldRecovery- Removal-SI/Crosstalk Analysis.	[9]
Practical: 1. Design and verification of Digital Architecture for given specification 2. Timing constraints development of Digital Architecture 3. Logical Synthesis of Digital Architecture 4. Pre-layout timing check of Digital Architecture 5. RTL to gate of Digital Architecture 6. Floorplan of Digital Architecture 7. Placement of Digital Architecture 8. CTS of Digital Architecture	[30]
Total Hours: (Lecture - 45; Practical - 30)	**75**

Text Book(s):

1.	Michael John Sebastian Smith, Application-Specific Integrated Circuits, 2002, First Edition, Addison Wesley.
2.	Himanshu Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys® Design Compiler™ and PrimeTime®, Kluwer Academic Publishers,2013 .

Reference(s):

1.	J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, 2010, First Edition, Springer, USA.
2.	Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, 2021, First Edition, Springer, Singapore.
3.	Shivananda R and Veena S, SoC Physical Design: A Comprehensive Guide, 2022, First Edition, Springer.
4.	Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs: A Practical Approach”, Prentice Hall PTR, 2003.

*SDG 9 – Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Floor Planning**	
1.1	Overview of Physical Design flow	1
1.2	Floorplanning Goals and Objectives	1
1.3	Measurement of Delay in Floorplanning	2
1.4	Floorplanning Tools	1
1.5	Channel Definition	2
1.6	I/O and Power Planning, Clock Planning.	1
2.0	**Placement**	
2.1	Placement Goals and Objectives	1
2.2	Placement Algorithms	1
2.3	Eigenvalue Placement	1
2.4	Iterative Placement Improvement	1
2.5	Placement Using Simulated Annealing	1
2.6	Timing-driven floorplanning	2
2.7	placement design flow	1
2.8	Information Formats	1
3.0	**Routing**	
3.1	Global Routing: Goals and Objectives, Measurement of Interconnect Delay	1
3.2	Global Routing Methods, Global Routing Between Blocks	1
3.3	Global Routing Inside Flexible Blocks, Timing-Driven Methods	1
3.4	Back-annotation, Detailed Routing: Goals and Objectives	1
3.5	Measurement of Channel Density, Algorithms-Left-Edge Algorithm	1
3.6	Constraints and Routing Graphs	1
3.7	Area-Routing Algorithms, Multilevel Routing	2
4.0	**Timing Analysis**	
4.1	Timing Parameter Definition	1
4.2	Setup Timing Check- Hold Timing Check	2
4.3	Multicycle PathsHalf-Cycle Paths	2
4.4	False Paths	1
4.5	Clock skew	1
4.6	Setup and Hold Violation Fixing	1
4.7	Origins of Clock Skew/Jitter and impact on Performance.	1
5.0	**Signoff Checks**	
5.1	Physical Design Verification	1
5.2	Signoff DRC	2
5.3	LVS Timing Signoff	2
5.4	DRV Checks-Setup	2
5.5	Hold Recovery, Removal-SI/Crosstalk Analysis	2
1	**Practical:**	
2	Design and verification of Digital Architecture for given specification	3
3	Timing constraints development of Digital Architecture	4
4	Logical Synthesis of Digital Architecture	4
5	Pre-layout timing check of Digital Architecture	4
6	RTL to gate of Digital Architecture	3
7	Floorplan of Digital Architecture	4
8	Placement of Digital Architecture	4

Course Designer(s)

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Chairman - Board of Studies
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60 EV 604	Analog and Digital Communication	Category	L	T	P	Credit
		PC	3	1	0	4

Objectives

- To explain the concept of electronic communication system
- To discuss the amplitude and frequency modulation techniques
- To compare the pulse analog and pulse digital modulation techniques
- To explain the different digital modulation and demodulation principles
- To discuss the spread spectrum modulation techniques

Pre-requisites

- Signals and System

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the concept of electronic communication system	Understand
CO2	Discuss the amplitude and frequency modulation techniques	Understand
CO3	Compare the pulse analog and pulse digital modulation techniques	Analyse
CO4	Explain the different digital modulation and demodulation principles	Understand
CO5	Discuss the spread spectrum modulation techniques	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	40	60
Apply	-	-	-
Analyse	-	10	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 604–Analog and Digital Communication

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	1	0	60	4	40	60	100

Communication Systems* Elements of Communication System, Technologies in Communication Systems, Signal Representation and Analysis, Analog and Digital Messages, Channel Effect, SNR and System Capacity, Modulation and Detection, Need for Modulation, Noise - External noise, Internal noise, Noise calculations, Noise figure, Noise temperature.	[9]
Analog Modulation Techniques* Amplitude Modulation techniques - Elements of Analog Communication, Amplitude modulation techniques, Generation of AM signals. Angle modulation techniques - Theory of Angle Modulation techniques, Practical Issues in FM, Generation of FM.	[9]
Pulse Modulation* Types of Pulse Modulation Techniques - PAM, PWM and PPM, Comparison between PAM, PWM & PPM. Comparison of FDM and TDM, Pulse Code Modulation - Generation and Reconstruction, Quantization Noise, Non-Uniform Quantization and Companding. DPCM, Adaptive DPCM, DM, Adaptive DM, Noise in PCM and DM.	[9]
Digital Modulation Techniques* ASK Modulator, Coherent ASK Detector, FSK Modulator, Non-Coherent FSK Detector, BPSK Modulator, Coherent BPSK Detection, Principles of QPSK, Differential PSK and QAM.	[9]
Spread Spectrum Communications* Frequency Hopping Spread Spectrum Techniques, Direct sequence Spread Spectrum Techniques, CDMA, Latest trends in digital communication.	[9]
Total Hours: (Lecture - 45; Tutorial - 15)	**60**

Text Book(s):

1. Lathi B.P. and Zhi Ding, “Modern Digital and Analog Communication Systems”, Oxford University Press, Fourth Edition, 2011.
2. Simon Haykin and Michael Moher, “Communication systems”, John Wiley & Sons, Fifth Edition, 2016.

Reference(s):

1. Simon Haykin, “An Introduction to Analog and Digital Communications”, John Wiley & Sons, 2015.
2. Dennis Roddy and John Coolen, “Electronic Communications”, Pearson, Fourth Edition, 2014.
3. Sam Shanmugam, “Digital and Analog Communication Systems”, 2nd ed, John Wiley, 2019
4. George Kennedy, Bernard Davis and S R M Prasanna, “Electronic Communication Systems”, Tata McGraw Hill, Fifth Edition, 2011.

*SDG 9 – Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Communication Systems**	
1.1	Elements of Communication System	1
1.2	Technologies in Communication Systems	1
1.3	Signal Representation and Analysis	1
1.4	Analog and Digital Messages	1
1.5	Channel Effect, SNR and System Capacity	1
1.6	Modulation and Detection, Need for Modulation	1
1.7	Noise - External noise, Internal noise	1
1.8	Noise calculations	1
1.9	Noise figure, Noise temperature	1
2.0	**Analog Modulation Techniques**	
2.1	Amplitude Modulation techniques	1
2.2	Elements of Analog Communication	1
2.3	Generation of AM signals	1
2.4	Angle modulation techniques	2
2.5	Theory of Angle Modulation techniques	2
2.6	Practical Issues in FM	1
2.7	Generation of FM	1
3.0	**Pulse Modulation**	
3.1	Types of Pulse Modulation Techniques - PAM	1
3.2	PWM	1
3.3	PPM	1
3.4	Comparison between PAM, PWM & PPM	1
3.5	Comparison of FDM and TDM	1
3.6	Pulse Code Modulation - Generation and Reconstruction	1
3.7	Quantization Noise, Non-Uniform Quantization and Companding	1
3.8	DPCM, Adaptive DPCM	1
3.9	DM, Adaptive DM, Noise in PCM and DM	1
4.0	**Digital Modulation Techniques**	
4.1	ASK Modulator	1
4.2	Coherent ASK Detector	1
4.3	FSK Modulator	1
4.4	Non-Coherent FSK Detector	1
4.5	BPSK Modulator	1
4.6	Coherent BPSK Detection	1
4.7	Principles of QPSK	1
4.8	Differential PSK and QAM	2
5.0	**Spread Spectrum Communications**	
5.1	Frequency Hopping Spread Spectrum Techniques	3
5.2	Direct sequence Spread Spectrum Techniques	3
5.3	CDMA	2
5.4	Latest trends in digital communication	1

Course Designer(s)

1. Dr.P.Kumar – kumar@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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60 MY 004	Disaster Management	Category	L	T	P	Credit
		MC	2	0	0	0

Objectives

- To understand the fundamental concepts of disasters, including hazard, vulnerability, risk, and capacity
- To recognise the different types of natural, biological, technological, and man-made disasters
- To explain the disaster management cycle and apply appropriate strategies for prevention, mitigation, preparedness, response, recovery, and rehabilitation.
- To know the disaster management frameworks and practices in India
- To recognise science, technology, and engineering approaches for disaster risk reduction

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand basic terms related to disasters, hazards, vulnerability, risk, and disaster management.	Understand
CO2	Recognize different types of natural, biological, technological, and man-made disasters.	Understand
CO3	Know the main stages of the disaster management cycle and the roles of people and authorities during disasters.	Understand
CO4	Summarize the disaster management systems, laws, and institutions in India.	Understand
CO5	Recognize the role of safety practices, science, and technology in reducing disaster risks.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	1	-	-	-	-	1	-	-	-	-	-	-	-	-	-
CO2	1	1	-	-	-	1	1	-	-	-	-	-	-	-	-
CO3	1	1	-	-	-	2	1	-	-	-	-	-	-	-	-
CO4	-	-	-	-	-	2	2	-	-	-	-	-	-	-	-
CO5	-	-	-	-	1	2	2	-	-	-	-	-	-	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	-
Understand	40	40	-
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	-

Passed in BoS Meeting held on 20/12/2025
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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 MY 004 - Disaster Management

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	2	0	0	30	0	100	-	-

Understanding Disasters Understanding the Concepts and definitions of Disaster, Hazard, Vulnerability, Risk, Capacity – Disaster and Development, and disaster management	[6]
Types, Trends, Causes, Consequences and Control of Disasters Geological Disasters (earthquakes, landslides, tsunami, mining) Hydro-Meteorological Disasters (floods, cyclones, lightning, thunder-storms, hail storms, avalanches, droughts, cold and heat waves) Biological Disasters (epidemics, pest attacks, forest fire) Technological Disasters (chemical, industrial, radiological, nuclear) and Man- made Disasters (building collapse, rural and urban fire, road and rail accidents, nuclear, radiological, chemicals and biological disasters) Global Disaster Trends – Emerging Risks of Disasters – Climate Change and Urban Disasters	[6]
Disaster Management Cycle and Framework Disaster Management Cycle – Paradigm Shift in Disaster Management Pre-Disaster – Risk Assessment and Analysis, Risk Mapping, zonation and Microzonation, Prevention and Mitigation of Disasters, Early Warning System; Preparedness, Capacity Development Awareness During Disaster – Evacuation – Disaster Communication – Search and Rescue - Emergency Operation Centre – Incident Command System – Relief and Rehabilitation – Post-disaster – Damage and Needs Assessment, Restoration of Critical Infrastructure – Early Recovery – Reconstruction and Redevelopment; IDNDR, Yokohama Strategy, Hyogo Framework of Action	[6]
Disaster Management in India Disaster Profile of India – Mega Disasters of India and Lessons Learnt Disaster Management Act 2005 – Institutional and Financial Mechanism National Policy on Disaster Management, National Guidelines and Plans on Disaster Management; Role of Government (local, state and national), Non-Government and Inter- Governmental Agencies	[6]
Applications of Science and Technology for Disaster Management Geo-informatics in Disaster Management (RS, GIS, GPS and RS) Disaster Communication System (Early Warning and Its Dissemination) Land Use Planning and Development Regulations Disaster Safe Designs and Constructions Structural and Non-Structural Mitigation of Disasters S&T Institutions for Disaster Management in India.	[6]
Total Hours:	**30**

Text Book(s):

1.	Coppola D P, 2007. Introduction to International Disaster Management, Elsevier Science (B/H), London.
2.	Manual on natural disaster management in India, M C Gupta, NIDM, New Delhi

Reference(s):

1.	An overview on natural & man-made disasters and their reduction, R K Bhandani, CSIR, New Delhi
2.	World Disasters Report, 2009. International Federation of Red Cross and Red Crescent, Switzerland
3.	Encyclopaedia of disaster management, Vol I, II and IIIL Disaster management policy and administration, S L Goyal, Deep & Deep, New Delhi, 2006
4.	Disasters in India Studies of grim reality, Anu Kapur & others, 2005, 283 pages, Rawat Publishers, Jaipur

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**Understanding Disasters – Basic Concepts**	
1.1	Introduction to Disaster: Concepts and Definitions of Disaster and Hazard	1
1.2	Vulnerability, Risk, and Capacity – Relationships and Examples	1
1.3	Disaster and Development – Link between Development and Disasters	1
1.4	Types of Vulnerabilities (Physical, Social, Economic, Environmental)	1
1.5	Introduction to Disaster Management: Meaning, Objectives and Scope	1
1.6	Case studies and discussion on Disaster Management concepts	1
2.0	**Types of Disasters**	
2.1	Geological Disasters: Earthquakes, Landslides, Tsunami, Mining Disasters	1
2.2	Hydro-Meteorological Disasters: Floods, Cyclones, Lightning, Thunderstorms	1
2.3	Hydro-Meteorological (continued): Hail storms, Avalanches, Droughts, Heat & Cold waves	1
2.4	Biological Disasters: Epidemics, Pest attacks, Forest fires	1
2.5	Technological & Man-made Disasters: Chemical, Industrial, Nuclear, Radiological, Accidents	1
2.6	Global Disaster Trends, Emerging Risks, Climate Change and Urban Disasters	1
3.0	**Disaster Management Cycle and Framework**	
3.1	Disaster Management Cycle and Paradigm Shift	1
3.2	Pre-Disaster: Risk Assessment, Risk Mapping, Zonation & Microzonation	1
3.3	Prevention, Mitigation, Early Warning System, Preparedness, Capacity Building	1
3.4	During Disaster: Evacuation, Disaster Communication, Search & Rescue	1
3.5	Emergency Operation Centre (EOC), Incident Command System, Relief & Rehabilitation	1
3.6	Post-Disaster: Damage Assessment, Recovery, Reconstruction, IDNDR, Yokohama, Hyogo Framework	1
4.0	**Disaster Management in India**	
4.1	Disaster Profile of India and Vulnerability Analysis	1
4.2	Mega Disasters in India and Lessons Learnt	1
4.3	Disaster Management Act 2005 – Features and Provisions	1
4.4	Institutional and Financial Mechanism for Disaster Management	1
4.5	National Policy, National Guidelines and Disaster Management Plans	1
4.6	Role of Government (Local, State, National), NGOs and International Agencies	1
5.0	**Applications of Science and Technology for Disaster Management**	
5.1	Geo-informatics: Remote Sensing, GIS and GPS in Disaster Management	1
5.2	Disaster Communication Systems and Early Warning Dissemination	1
5.3	Land Use Planning and Development Regulations	1
5.4	Disaster Safe Design and Construction Practices	1
5.5	Structural and Non-Structural Mitigation Measures	1
5.6	Science & Technology Institutions for Disaster Management in India	1

Course Designer(s)

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Passed in BoS Meeting held on 20/12/2025
Approved in Academic Council Meeting held on 03/01/2026

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 6P1	VLSI Verification and Testing Laboratory	Category	L	T	P	Credit
		PC	0	0	3	1.5

Objectives

- To understand the knowledge and skills necessary to comprehensively analyse and verify the output of combinational logic circuits
- To inculcate the knowledge and skills required to thoroughly analyse and verify the output of sequential logic circuits
- To learn to apply coverage - driven verification methodologies to guide and optimize the verification effort in digital design projects
- To gain a comprehensive understanding of fault simulation techniques used to model faults in digital circuits
- To equip students with the knowledge and skills necessary to perform logic equivalence checks (formal verification) between two digital designs

Pre-requisites

- NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Analyse and verify the output of all combinational logic circuits with all input combinations	Analyse
CO2	Analyse and verify the output of all sequential logic circuits with all input combinations	Analyse
CO3	Apply coverage - driven verification methodologies to guide and optimize the verification effort.	Apply
CO4	Simulate faults and analyse the fault coverage achieved by the generated test patterns.	Analyse
CO5	Perform logic equivalence checks using formal verification tools and techniques.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	3	3	3	-	3	3	3	-
CO2	3	3	3	3	3	-	-	3	3	3	-	3	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	3	-
CO4	3	3	3	3	3	-	-	3	3	3	-	3	3	3	-
CO5	3	3	3	3	3	-	-	3	3	3	-	3	3	3	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	-	-
Apply	25	12	50	50
Analyse	25	13	50	50
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	50	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 6P1 - VLSI Verification and Testing Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VI	0	0	3	45	1.5	60	40	100

List of Experiments*:

1. Development of an Exhaustive Test Bench for the 1 - Bit Full Adder.
2. Development of Exhaustive Test Bench for 16X1 Multiplexer Using File Reading Writing Features.
3. Development of Layered Test Bench Components for Functional Verification of an 8-Bit Full Adder.
4. Development of Layered Test Bench Components for Functional Verification of a Counter.
5. Development of Layered Test Bench Components for Functional Verification of 8 - Bit ALU.
6. Development of Layered Test Bench Components for Functional Verification of Synchronous FIFO.
7. Development of Layered Test Bench Components for Functional Verification of Round Robin Arbiter.
8. Analysis of Code Coverages and Write Development of Functional Coverage.
9. Design for Test and Automatic Test Pattern Generation for a 4 - Bit Counter.
10. Perform the Logic Equivalence (Formal Verification).

Lab Manual	
1.	"VLSI Verification and Testing Laboratory", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 9 – Industry Innovation and Infrastructure

Course Designer(s)

1. Mr S.Pradeep – pradeeps@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 6P2	Embedded Systems Laboratory	Category	L	T	P	Credit
		PC	0	0	3	1.5

Objectives

- To familiarize the operators and registers in Embedded C
- To learn about ADC and DAC
- To interface peripherals and processors associated with embedded systems
- To understand the concept of UART communication
  To familiarize with RTOS in Embedded computing

Pre-requisites

- Microprocessors and Microcontrollers, Basics of C Programming

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop bare metal Embedded C programs to perform transmission and reception.	Apply
CO2	Develop Embedded C programs for interfacing peripherals	Apply
CO3	Develop multitasking bare metal Embedded C programs using RTOS	Apply
CO4	Implement Embedded C programs for interfacing DC motors	Apply
CO5	Create applications utilizing timers or external interrupts with PWM, and SPI interfaces	Evaluate

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	2	3
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	2	3
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	2	3
CO4	3	3	3	3	3	-	-	3	3	3	3	3	3	2	3
CO5	3	3	3	3	3	-	-	3	3	3	3	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model Examination (Marks)	End Sem Examination (Marks) Lab
	Lab	Activity		
Remember	-	-	-	-
Understand	-	-	-	-
Apply	50	-	100	50
Analyse	-	-	-	-
Evaluate	-	25	-	-
Create	-	-	-	-
Total	50	25	100	50

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 6P2 - Embedded Systems Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VI	0	0	3	45	1.5	60	40	100

List of Experiments:

1. Develop a bare metal Embedded C program to access GPIO ports *
2. Develop a bare metal Embedded C program to perform UART transmission and reception
3. Develop the bare metal Embedded C program for ADC and print the value in UART
4. Develop the bare metal Embedded C program for ADXL345 Accelerometer using the I2C *
5. Develop the multitasking bare metal Embedded C program using free RTOS for following task
   - Task-1: Blink LED for 1 second (using Vtask timer)
   - Task-2: Read ADXL345 print in UART
   - Task-3: Read ADC and trigger an LED once threshold meets and print the value in UART
6. Develop the bare metal Embedded C program for DC motor interface

Open ended experiments:

1. Develop an application using timer or external interrupts and PWM **
2. Develop an application using SPI interface

Lab Manual

1.	"Embedded Systems Laboratory", Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 9 – Industry Innovation and Infrastructure

**SDG 7 – Affordable and Clean Energy

Course Designer(s)

1. Mr.T.Rajavenkatesan-rejavenkatesan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 6P3	Design Thinking and Product Development Laboratory	Category	L	T	P	Credit
		PC	0	0	2	1

Objectives

- Ideate and develop innovative solutions for the given problem statement
- Develop soft prototype and visualize user scenarios for early-stage product validation
- Develop medium and hard prototype, integrating technical, ergonomic, and aesthetic considerations
- Conduct testing, gather user feedback, and apply iterative design processes
- Document, publish and present their solution

Pre-requisites

- Design Thinking and Innovation Laboratory

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Generate innovative solutions to address specific problem statements.	Apply
CO2	Create and evaluate soft prototype, including paper prototypes and storyboards, to test initial design concepts.	Create
CO3	Create medium and hard prototype using 3D modelling and printing, incorporating human factors and system design.	Create
CO4	Perform usability studies, analyze user feedback, and iterate their designs to finalize user-centered solutions.	Analyse
CO5	Prepare professional documentation, and deliver a comprehensive project report and presentation.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	2	3	3	3	3	3	-	3	3	3	3
CO2	3	3	3	-	-	-	-	3	3	3	-	-	3	3	3
CO3	3	3	3	3	3	-	-	3	3	3	-	-	3	3	3
CO4	3	3	3	3	3	3	3	3	3	3	-	3	3	3	3
CO5	3	-	-	-	-	-	-	3	3	3	3	-	3	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Review I (CO1)			Review II (CO2,CO3)			Review III (CO4)			(R1+R2+R3)	Internal Marks
Generating Creative ideas	Concept Maps and Evaluation	Presentation	Soft Prototyping	Hi-fidelity prototyping	Demonstration	User Studies & Feedback	Finalise solution	Presentation	Total	
10	10	10	10	20	10	10	10	10	**100**	**60**

Report and Presentation (CO1, CO2, CO3,CO4 & CO5)				External Marks
Report	Presentation	Demonstration	Total	
50	30	20	**100**	**40**

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K.S.Rangasamy College of Technology – Autonomous R 2022							
B.E – Electronics Engineering (VLSI Design & Technology)							
60 EV 6P3 – Design Thinking and Product Development Laboratory							
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**	
	L	T	P		C	CA	ES	Total
VI	0	0	2	30	1	60	40	100

Ideation Generating Creative ideas - Idea Sketching, Brainstorming for Ideas, SCAMPER, Creativity and Lateral thinking- Concept Maps and Evaluation	[8]
Soft Prototyping Soft Prototyping - Paper Prototype (low-fidelity), Scenarios and Storyboarding, MVP (minimum Viable product).	[4]
Final Prototyping Medium Prototyping - Proof of Concept (PoC), Info Architecture, Experience Design- Human Factors / Ergonomics - Systems Mapping – high prototyping - 3D Modelling & Printing.	[6]
Usability Studies User Studies – Observation – Conversations - Think-aloud protocol – Feedback – Iterate - Finalise solution.	[8]
Publish the solution Publish the ideas: Journal Publication & Intellectual Property Rights–Prepare project report and present the final solution.	[4]
Total Hours:	30

Reference(s):

1.	NPTEL: Design Thinking and Innovation by Prof. Ravi Poovaiah, IDC School of Design, IIT Bombay. https://onlinecourses.swayam2.ac.in/aic23_ge17/preview, https://dsource.in/dti.
2.	NPTEL: Innovation by Design by Prof. B. K. Chakravarthy, IDC School of Design, IIT Bombay, https://onlinecourses.swayam2.ac.in/aic19_de02/preview.
3..	www.dsource.in , The Resource for Design by e-Kalpa Design Team,IDC, IIT Bombay, DoD, IIT Guwahati & NID, Bengaluru

SDG 9 – Industry Innovation and Infrastructure

Course Designer(s)

1. Dr.K.Raja – raja@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 CG 0P5	Comprehension Test	Category	L	T	P	Credit
		CG	0	0	2	1*

Objectives

- To evaluate the knowledge gained in core courses relevant to the programme of study
- To assess the technical skill in solving complex engineering problems

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Infer knowledge in their respective programme domain.	Apply
CO2	Attend interviews for career progression.	Apply
CO3	Exhibit professional standards to solve engineering problems.	Apply
CO4	Promote holistic approach to problem solving.	Apply
CO5	Examine the competency of graduates in specific programme domain.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	2	-	-	-	-	1	2	2	3	-	-	-
CO2	3	3	2	2	-	-	-	-	1	2	2	3	-	-	-
CO3	3	3	2	2	-	-	-	-	1	2	2	3	-	-	-
CO4	3	3	2	2	-	-	-	-	1	2	2	3	-	-	-
CO5	3	3	2	2	-	-	-	-	1	2	2	3	-	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

The overall knowledge of the candidate in various courses he/she studied shall be evaluated with multiple choice questions.

*SDG: 4- Quality Education

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

SEVENTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EV 701	Introduction to Microfabrication	2	40	60	100	45	100
2.	60 EV 703	Electronic Packaging	2	40	60	100	45	100
3.	60 EV E4*	Professional Elective IV	2	40	60	100	45	100
4.	60 AC 001	Research Skill Development	1	100	00	100	00	100
THEORY CUM PRACTICAL								
5.	60 EV 702	Verification Methodologies and Bus Architectures	2	50	50	100	45	100
6.	60 EV E3*	Professional Elective III	2	50	50	100	45	100
7.	60 AB 00*	NCC\NSS\NSO\ YRC\RRC\Yoga \Fine Arts	2	50	50	100	45	100
PRACTICAL								
8.	60 EV 7P1	Microfabrication Laboratory	3	60	40	100	45	100
9.	60 EV 7P2	Project Work Phase - I	3	60	40	100	45	100
10.	60 CG 0P6	Internship	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination, 50 marks for theory cum practical End Semester Examination and 40 marks for practical End Semester Examination.

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
Department of Electronics Engineering
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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV 701	Introduction to Microfabrication	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To understand the fundamentals of microfabrication, micro metrology, and materials characterization techniques.
- To gain proficiency in basic microfabrication processes, including lithography, etching, wafer preparation, and thermal processes.
- To learn techniques for creating micro- and nano-scale structures, focusing on various etching, deposition, and metallization methods.
- To understand process integration for CMOS, BICMOS, and MEMS technologies, with a focus on layout, design rules, and isolation techniques.
- To explore MEMS design and fabrication, including material properties, micromachining, bonding, and the creation of micro sensors and actuators.

Pre-requisites

- Basics of physics and chemistry
- Basics of electronic Devices and Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the foundational knowledge of microfabrication, metrology, and materials testing, applying these concepts in device development.	Apply
CO2	Apply lithography, etching, bonding, and layer transfer techniques, understanding their roles in microfabrication processes.	Apply
CO3	Create and characterize micro- and nano-scale structures, utilizing self-aligned, plasma-etched, and sacrificial-release techniques.	Apply
CO4	Apply CMOS, BICMOS, and MEMS fabrication knowledge, integrating design rules and isolation techniques in layout and design.	Apply
CO5	Design and fabricate MEMS devices, including micro sensors and actuators, utilizing micromachining and wafer bonding techniques.	Apply

Mapping with Programme Outcomes

COs	POs											PSOs			
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	2	2	-	-	1	-	-	-	2	3	3	1
CO2	3	3	3	3	2	-	-	1	-	-	-	1	3	2	1
CO3	3	3	3	2	2	-	-	1	-	-	-	2	2	3	3
CO4	3	3	3	3	2	-	-	3	-	-	-	1	3	3	1
CO5	3	3	3	3	3	-	-	3	-	-	-	3	3	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	40	40	60
Apply	10	10	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV 701 – Introduction to Microfabrication

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Microfabrication* Microfabrication - Materials – Micro metrology - Materials Characterization – Simulation – Silicon – Thin Film Materials and Processes – Epitaxial Growth – Thin Film Growth and Structure.	[9]
Basic Processes* Lithography – Pattern Generation – Optical Lithography – Lithographic Patterns – Etching – Wafer Cleaning and Surface Preparation – Thermal Oxidation – Diffusion – Ion Implantation – Chemical and Mechanical Polishing – Bonding and Layer Transfer – Moulding and Stamping.	[9]
Structures* Self-aligned structures – Plasma etched Structures – Wet etched structures – Sacrificial and Relesed Structures – Structures by Deposition –Interconnects and Contacts - Metallization – Assembly – Packaging and Yield.	[9]
Process Integration* CMOS Consideration - MOS Transistor layout – Design rules – CMOS fabrication Technology – Silicon on Insulator – Bipolar Process Integration – Isolation Techniques – BICMOS.	[9]
MEMS* Mechanical Properties – Micromachining – Etchants – Wafer Bonding – IC Process Compatibility - Processing of non-silicon substrates - Micro Sensors and Actuators - Capacitive Accelerometer, Piezoresistive Pressure Sensor, Electrostatic Comb-Drive, Magnetic Micro relay	[9]
Total Hours:	45

Text Book(s):	
1.	Sami Fransiila, “Introduction to Micro Fabrication”, John Wiley & Sons, Second Edition,2010.
2.	Richard Jaeger, “Introduction to Micro Electronic Fabrication”, Prentice Hall, Second Edition,2002.
Reference(s):	
1.	Madou, M. J.” Fundamentals of microfabrication”, Boca Raton, FL: CRC Press,2nd Edition,2002.
2.	Sze, S. M., & Kwok, K. N.” Physics of semiconductor devices”, Hoboken, NJ: Wiley,3rd Edition,2006.
3.	Sze, S. M. “VLSI technology”, New York, NY: McGraw-Hill,2nd Edition,2000.
4.	Sorab Ghandhi,” VLSI Fabrication Principles (Silicon and Gallium Arsenide)”, John Wiley & Sons, Second Edition, 1994.

*SDG 9 - Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Microfabrication**	
1.1	Microfabrication	1
1.2	Materials and Micro metrology	1
1.3	Materials Characterization	1
1.4	Simulation	1
1.5	Silicon Process	1
1.6	Thin Film Materials and Processes	1
1.7	Thin Film Materials and Processes	1
1.8	Epitaxial Growth	1
1.9	Thin Film Growth and Structure.	1
2.0	**Basic Processes**	
2.1	Lithography and Pattern Generation	1
2.2	Optical Lithography and Lithographic Patterns	1
2.3	Etching	1
2.4	Wafer Cleaning and Surface Preparation	1
2.5	Thermal Oxidation	1
2.6	Diffusion and Ion Implantation	1
2.7	Chemical and Mechanical Polishing	1
2.8	Bonding and Layer Transfer	1
2.9	Moulding and Stamping.	1
3.0	**Structures**	
3.1	Self-aligned structures	1
3.2	Self-aligned structures	1
3.3	Plasma etched Structures	1
3.4	Wet etched structures	1
3.5	Sacrificial and Relesed Structures	1
3.6	Sacrificial and Relesed Structures	1
3.7	Structures by Deposition	1
3.8	Interconnects and Contacts, Metallization	1
3.9	Assembly Packaging and Yield	1
4.0	**Process Integration**	
4.1	CMOS Consideration	1
4.2	MOS Transistor layout & Design rules	1
4.3	CMOS fabrication Technology	1
4.4	CMOS fabrication Technology	1
4.5	Silicon on Insulator	1
4.6	Bipolar Process Integration	1
4.7	Bipolar Process Integration	1
4.8	Isolation Techniques	1
4.9	BICMOS	1
5.0	**MEMS**	
5.1	Mechanical Properties and Micromachining	1
5.2	Etchants	1
5.3	Wafer Bonding and IC Process Compatibility	1
5.4	Processing of non-silicon substrates	1
5.5	Micro Sensors and Actuators	1
5.6	Capacitive Accelerometer	1
5.7	Piezoresistive Pressure Sensor	1
5.8	Electrostatic Comb-Drive	1
5.9	Magnetic Micro relay	1

Course Designer(s)

1. Mr.T. Rajavenkatesan – rajavenkatesan@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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Tiruchengode - 637 215

60 EV 702	Verification Methodologies and Bus Architectures	Category	L	T	P	Credit
		PC	3	0	2	4

Objectives

- To provide the students, with a complete understanding of uvm testing
- To become proficient at UVM verification
- To know about the verification components used and to build it
- To describe the register layer classes and to generate it
- To learn all peripheral bus test benches and its advanced level

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Demonstrate proficiency in developing reusable verification components	Apply
CO2	Discuss the transaction-level modeling (TLM) techniques	Understand
CO3	Construct UVM test benches for functional verification	Apply
CO4	Utilize UVM register layer classes for register verification	Understand
CO5	Design and implement test benches for advanced peripheral bus (APB) protocol	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-

3 - Strong; 2 - Medium; 1 – Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Exam (Marks)	End Sem Examination (Marks)	
	1		2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	-	-	-	-	20	20	20
Understand	30	40	30	40	60	60	60
Apply	30	60	30	60	20	20	20
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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Tiruchengode - 637 215

Syllabus								
K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 702 - Verification Methodologies and Bus Architectures								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	3	0	2	75	4	50	50	100

UVM and TLM* The Typical UVM Testbench Architecture - The UVM Class Library-Transaction - Level Modeling (TLM) – Overview - TLM, TLM-1, and TLM - 2.0 -TLM-1 Implementation- TLM - 2.0 Implementation.	[9]
Developing Reusable Verification Components* Modeling Data Items for Generation – Transaction - Level Components - Creating the Driver – Creating the Sequencer - Connecting the Driver and Sequencer - Creating the Monitor - Instantiating Components Creating the Agent - Creating the Environment - Enabling Scenario Creation - Managing of Test Implementing Checks and Coverage	[9]
UVM using Verification Components* Creating a Top - Level Environment - Instantiating Verification Components - Creating Test Classes - Verification Component Configuration - Creating and Selecting a User - Defined Test – Creating Meaningful Tests - Virtual Sequences - Checking for DUT Correctness – Scoreboards - Implementing a Coverage Model. Integrating Functional Coverage into UVM Testbench.	[9]
UVM using the Register Layer Classes* Using The Register Layer Classes – Back - Door Access - Special Registers - Integrating a Register Model in a Verification Environment - Integrating a Register Model - Randomizing Field Values - Pre Defined Sequences.	[9]
Assignment in Test benches* Assignment, Advanced Peripheral Bus (APB): Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.	[9]
Practical: 1. TLM Implementation. 2. Modelling Data items for Generation. 3. Write UVM test bench for digital logic circuits. 4. Write UVM for Special Registers. 5. Test Bench for Testing Driver and Sequencer. **6.** Implementation of APB protocol.	[30]
Total Hours: (Lecture - 45; Practical - 30)	**75**
Text Book(s):	

1.	Sharon Rosenberg, Kathleen Meade “A Practical Guide to Adopting the Universal Verification Methodology (UVM)” Cadence Design Systems, 2010
2.	Ray Salemi, “The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology”, Boston Light Press, 2013
Reference(s):	
1.	https://www.accellera.org/images/downloads/standards/uvm/uvm_users_guide_1.1.pdf
2.	https://www.udemy.com/course/learn-ovm-uvm/
3.	http://www.testbench.in/ot_00_index.html
4.	http://www.testbench.in/UT_00_INDEX.html

*SDG:4- Quality Education

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**UVM and TLM**	
1.1	The Typical UVM Testbench Architecture	1
1.2	The UVM Class Library	2
1.3	Transaction-Level Modeling (TLM)	2
1.4	TLM-1 & TLM-2.0	2
1.5	TLM-1 Implementation	1
1.6	TLM-2.0 Implementation.	1
2.0	**Developing Reusable Verification Components**	
2.1	Modeling Data Items for Generation	1
2.2	Transaction-Level Components	1
2.3	Creating the Driver, Creating the Sequencer	1
2.4	Connecting the Driver and Sequencer	1
2.5	Creating the Monitor, Instantiating Components	1
2.6	Creating the Agent	1
2.7	Creating the Environment	1
2.8	Enabling Scenario Creation	1
2.9	Managing of Test Implementing Checks and Coverage	1
3.0	**UVM using Verification Components**	
3.1	Creating a Top-Level Environment	1
3.2	Instantiating Verification Components, Creating Test Classes	1
3.3	Verification Component Configuration	1
3.4	Creating and Selecting a User-Defined Test	1
3.5	Creating Meaningful Tests	1
3.6	Virtual Sequences	1
3.7	Checking for DUT Correctness	1
3.8	Scoreboards- Implementing a Coverage Model	1
3.9	Integrating Functional Coverage into UVM Testbench.	1
4.0	**UVM using the Register Layer Classes**	
4.1	Using The Register Layer Classes	1
4.2	Back-Door Access	1
4.3	Special Registers	1
4.4	Integrating a Register Model in a Verification Environment	2
4.5	Integrating a Register Model	2
4.6	Randomizing Field Values	1
4.7	PreDefined Sequences	1
5.0	**Assignment in Test benches**	
5.1	Assignment, Advanced Peripheral Bus (APB): Protocol	2
5.2	Test bench Architecture	1
5.3	Driver and Sequencer	1
5.4	Monitor & Agent and Env	2
5.5	Creating Sequences , Building Test	2
5.6	Design and Testing of Top Module	1
	Practical:	
1	TLM Implementation.	4
2	Modelling Data items for Generation.	4
3	Write UVM test bench for digital logic circuits.	4
4	Write UVM for Special Registers.	4
5	Test Bench for Testing Driver and Sequencer.	6
6	Implementation of APB protocol.	6

Course Designer(s)

1. Mr S.Pradeep – pradeeps@ksrct.ac.in

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60 EV 703	Electronic Packaging	Category	L	T	P	Credit
		PC	3	0	0	3

Objectives

- To understand the fundamental concepts of electronic systems packaging
- To understand the packaging optimize materials for electronic systems
- To explore the knowledge of CAD for printed circuit board
- To illustrate the concepts of Surface Mount Technology and Thermal Management
- To study about the Embedded passive Technology

Pre-requisites

- Electronic Circuits and Embedded Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the electronic systems packaging	Understand
CO2	Describe the packaging optimize materials	Analyse
CO3	Design CAD for printed circuit board	Understand
CO4	Describe Surface Mount Technology and Thermal Management	Understand
CO5	Illustrate the Embedded passive Technology	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	40	50	60
Apply	-	-	-
Analyse	10	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2026								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV 703 - Electronic Packaging								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Electronic Systems Packaging * Definition of a System and History of Semiconductors, Products and Levels of Packaging, Packaging Aspects of Handheld Products, Definition of PWB, Basics of Semiconductor and Process Flowchart, Wafer Fabrication, Inspection and Testing, Wafer Packaging; Packaging Evolution; Chip Connection Choices, Wire Bonding, TAB and Flip Chip.	[9]
Semiconductor Packages * Single Chip Packages or Modules (SCM), Commonly Used Packages and Advanced Packages; Materials in Packages; Thermal Mismatch in Packages; Multichip Modules (MCM)-Types; System-in-Package (SIP); Packaging Roadmaps; Hybrid Circuits; Electrical Design Considerations In Systems Packaging, Resistive, Capacitive and Inductive Parasitic, Layout Guidelines and the Reflection Problem, Interconnection.	[9]
CAD for Printed Wiring Boards* Benefits From CAD; Introduction to DFM, DFR & DFT, Components of a CAD Package and Its Highlights - Circuit Design - Design for Reliability, Printed Wiring Board Technologies: Board - Level Packaging Aspects, Review of CAD Output Files for PCB Fabrication; Photo Plotting and Mask Generation, Process Flow-Chart; Vias; PWB Substrates; Surface Preparation, Photoresist and Application Methods; UV Exposure and Developing; Printing Technologies for PWBs, PWB Etching; Resist Stripping; Screen Printing Technology, Through-Hole Manufacture Process Steps; Panel and Pattern Plating Methods, Solder Mask for PWBs and Multilayer PWBs.	[9]
Surface Mount Technology and Thermal Considerations* SMD Benefits; Design Issues, Reflow and Wave Soldering Methods to Attach SMDs, Solders; Wetting of Solders; Flux and Its Properties; Defects In Wave Soldering, Vapour Phase Soldering, BGA Soldering and Desoldering/Repair; SMT Failures, SMT Failure Library and Tin Whisker, Tin-Lead and Lead-Free Solders; Phase Diagrams; Thermal Profiles for Reflow Soldering; Lead Free alloys, Lead-Free Solder Considerations; Green Electronics; Rohs Compliance and E-Waste Recycling, Issues, Thermal Design Considerations in Systems Packaging.	[9]
Embedded Passives Technology* Introduction to Embedded Passives; Need for Embedded Passives; Design Library; Embedded Resistor Processes, Embedded Capacitors; Processes for Embedding Capacitors; Case Study: Implementation of Embedded Passives Technology in Mobile Devices.	[9]
Total Hours:	45

Text Book(s):	
1.	Rao R. Tummala, “Fundamentals of Microsystems Packaging”, McGraw Hill, NY, 2001.
2.	R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011
Reference(s):	
1.	Tummala, Rao R, Microelectronics packaging handbook, McGraw Hill, 2008.
2.	William D. Brown, “Advanced Electronic Packaging”, IEEE Press, 1999.
3.	R.S.Khandpur, Printed Circuit Board, Tata McGraw Hill, 2005
4.	Bosshart, Printed Circuit Boards Design and Technology, TataMcGraw Hill, 1988

*SDG 9 – Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Overview of Electronic Systems Packaging**	
1.1	Definition of a system and history of semiconductors	1
1.2	Products and levels of packaging	1
1.3	Packaging aspects of handheld products	1
1.4	Definition of PWB	1
1.5	Basics of Semiconductor and Process flowchart	1
1.6	Wafer fabrication, inspection and testing	1
1.7	Wafer packaging; Packaging evolution	1
1.8	Chip connection choices	1
1.9	Wire bonding, TAB and flip chip	1
2.0	**Semiconductor Packages**	
2.1	Single chip packages or modules (SCM)	1
2.2	Commonly used packages and advanced packages	1
2.3	Materials in packages; Thermal mismatch in packages	1
2.4	Multichip modules (MCM)-types	1
2.5	System-in-package (SIP)	1
2.6	Packaging roadmaps Hybrid circuits	1
2.7	Electrical Design considerations in systems packaging	1
2.8	Resistive, Capacitive and Inductive Parasitics	1
2.9	Layout guidelines and the Reflection problem, Interconnection	1
3.0	**CAD for Printed Wiring Boards**	
3.1	Benefits from CAD; Introduction to DFM, DFR & DFT	1
3.2	Components of a CAD package and its highlights, Beginning a circuit design with schematic work and component layout	1
3.3	DFM check, list and design rules	1
3.4	Design for Reliability,Printed Wiring Board Technologies: Board-level packaging aspects, Review of CAD output files for PCB fabrication	1
3.5	Photo plotting and mask generation, Process flow-chart; Vias	1
3.6	PWB substrates; Surface preparation, Photoresist and application methods	1
3.7	UV exposure and developing; Printing technologies for PWBs, PWB etching; PWB etching, Resist stripping	1
3.8	Screenprinting technology, hrough-hole manufacture process steps; Panel and pattern plating methods, Solder mask for PWBs; Multilayer PWBs	1
3.9	Introduction to, microvias, Microvia technology and Sequential buildup technology process flow for high-density, interconnects	1
4.0	**SURFACE MOUNT TECHNOLOGY AND THERMAL CONSIDERATIONS**	
4.1	SMD benefits; Design issues; Introduction to soldering	1
4.2	Reflow and Wave Soldering methods to attach SMDs	1
4.3	Solders; Wetting of solders; Flux and its properties	1
4.4	Defects in wave soldering, Vapour phase soldering	1
4.5	BGA soldering and Desoldering/Repair; SMT failures	1
4.6	SMT failure library and Tin Whisker, Tin-lead and lead-free solders	1
4.7	Phase diagrams; Thermal profiles for reflow soldering; Lead freevAlloys	1
4.8	Lead-free solder considerations; Green electronics; RoHS	1
4.9	compliance and e-waste recycling, Issues, Thermal Design considerations in systems packaging	1
5.0	**EMBEDDED PASSIVES TECHNOLOGY**	
5.1	Introduction to embedded passives	1
5.2	Need for embedded passives	1
5.3	Design Library	1
5.4	Embedded resistor processes	1
5.5	Embedded capacitors	1
5.6	Processes for embedding capacitors	2
5.7	Case study examples	2

Course Designer(s)

1. Dr.S.Gomathi - gomathi@ksrct.ac.in

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60 EV 7P1	Micro Fabrication Laboratory	Category	L	T	P	Credit
		PC	0	0	4	2

Objectives

- To provide an understanding of how pattern transfer and dielectric layer formation are integrated in microfabrication.
- To explore the interactions between patterning and doping techniques in microfabrication.
- To simulate these processes, enabling students to evaluate their effects on device performance and quality.
- To enabling students to explore how these processes are applied to semiconductor fabrication and evaluate their effects on device performance and quality.
- Students will explore the micro-assembly and packaging processes and their effects on device performance and reliability.

Pre-requisites

- Basic Programming and Electron Devices and Circuits Concepts.

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Design and simulate the photolithography and oxidation process parameters to achieve high-resolution pattern transfer and precise control over dielectric layer formation.	Apply
CO2	Gain practical experience in optimizing etching and ion implantation parameters to achieve desired material removal and doping profiles.	Apply
CO3	Assess the effectiveness of cleaning processes in removing contaminants, such as particles or organic residues, which can affect the integrity and yield of fabricated devices.	Apply
CO4	Design, simulate, and optimize thin film deposition and wafer cleaning processes, understanding their critical role in achieving high-quality, reliable semiconductor devices.	Apply
CO5	Analyze the electrical behaviour of these devices by measuring their current-voltage (I-V) characteristics under different operating conditions.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Lab Experiments Assessment (Marks)		Model (Marks)	End Sem Examination (Marks)
	Lab	Activity		
Remember	-	-	-	-
Understand	25	12	50	50
Apply	25	13	50	50
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	-	-	-
Total	50	25	100	100

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K.S.Rangasamy College of Technology - Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 7P1 – Micro Fabrication Laboratory								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	0	0	4		60	60	40	100

List of Experiments*:

1. Design and simulate the photolithography process, including mask design, exposure, development, and pattern transfer onto a silicon wafer using TCAD tools and MATLAB.
2. Design and simulate the thermal oxidation process to grow silicon dioxide layers on a silicon wafer using TCAD.
3. Design and simulate both wet and dry etching processes for pattern transfer in microfabrication using TCAD.
4. Design and simulate the ion implantation process to introduce dopants (e.g., boron, phosphorus) into a silicon wafer using TCAD.
5. Design and simulate the deposition of thin films using Chemical Vapor Deposition (CVD) and sputtering techniques. Use TCAD tools to analyze the depth of dopant penetration and the profile of the doped regions in the silicon substrate.
6. Design and simulate wafer cleaning and contamination control methods in a cleanroom environment. Use TCAD tools to model the effect of cleaning techniques on the wafer surface and evaluate the removal of contaminants.
7. Design and simulate wafer bonding processes, such as anodic and fusion bonding, in microfabrication and analyze the model bonding stresses, alignment, and material properties, bond strength and reliability using TCAD.
8. Design and simulate the fabrication of microstructures using SU-8 photoresist in a photolithography process.
9. Design and simulate the fabrication of semiconductor devices (e.g., diodes, MOSFETs) and measure their I-V characteristics using TCAD.
10. Design and simulate the micro-assembly and packaging process for semiconductor devices using TCAD.

Lab Manual

1.	“Micro Fabrication Laboratory Manual”, Department of Electronics Engineering (VLSI Design and Technology), KSRCT.

*SDG 9 - Industry Innovation and Infrastructure

Course Designer(s)

1. Mr.T. Rajavenkatesan - rajavenkatesan@ksrct.ac.in

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60 EV 7P2	Project Work Phase - I	Category	L	T	P	Credit
		CG	0	0	4	2

Objectives

- To help the students apply their academic knowledge and technical skills in a specific domain
- To facilitate the students to identify, formulate and solve engineering problems
- To help the students design a system, component or process to meet the desired needs within realistic constraints
- To work and communicate efficiently in multidisciplinary terms
- To develop an understanding of professional and ethical responsibility in students

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Identify engineering problems in their domain of interest and carry out literature review in the chosen technical area	Understand
CO2	Analyse and identify an appropriate technique to solve the problem.	Analyse
CO3	Design engineering solution, do experimentation / simulation / programming / fabrication/ collect and interpret data utilizing a systems approach	Analyse
CO4	Communicate effectively in oral and written forms	Apply
CO5	Demonstrate the knowledge, skills and attitudes of a professional engineer as an individual and member of a team	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO2	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO5	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Review I (R1)			Review II (R2)		Review III (R3)			Total (R1+R2 +R3)	Internal
Literature Survey	Topic Identification & Justification	Work Plan	Approach	Conclusion	Demo-Existing System	Presentation	Report	Total	
10	10	10	20	20	10	10	10	100	100

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K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 7P2 - Project Work Phase - I								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	0	0	4	60	2	100	00	100

1. A committee is constituted with the project coordinator, project guide and HOD/Senior professor in the department
2. Three reviews have to be conducted by the committee
3. Problem should be selected by every batch of students
4. Students must do a literature survey collecting a minimum of 1 survey paper and 2 technical papers related to their work
5. Report has to be prepared by the students as per the format
6. Preliminary implementation can be done if possible Internal evaluation has to be done based on the three reviews for 100 marks

*SDG 4 – Quality Education

Course Designer(s)

1. Dr.P.Kumar-Kumar@ksrct.ac.in

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60 AB 001	NCC Studies (Air Wing) – I	Category	L	T	P	Credit
		HS	2	0	2	3

Objectives

- To designed especially for NCC Cadets to educate basic military knowledge
- To develop character, camaraderie, discipline, secular outlook
- To inculcate spirit of adventure, sportsman spirit
- To teach selfless service amongst cadets by working in teams
- To learn military subjects including weapon training and motivate them to join in tri-services

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Display sense of patriotism, secular values and shall be transformed into motivated youth who will carry out nation building through national unity and social cohesion	Remember
CO2	Demonstrate the sense of discipline with smartness and have basic knowledge of weapons and their use and handling	Remember
CO3	Illustrate various forces and moments acting on aircraft	Understand
CO4	Outline the concepts of aircraft engine and rocket propulsion	Understand
CO5	Design, build and fly chuck gliders/model airplanes and display static models	Create

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	3	3	3	3	3	-	-	-	-	3
CO2	-	-	-	-	3	-	-	-	-	-	-	-	-	-	3
CO3	3	2	1	1	-	-	-	-	-	-	-	-	-	-	3
CO4	3	2	1	1	-	-	-	-	-	-	-	-	-	-	3
CO5	3	2	1	1	-	-	-	-	-	-	-	-	-	-	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)			End Sem Examination (Marks)
	DST (20)	AM (20)	SBM (10)	
Remember	10	-	-	40
Understand	10	-	10	60
Apply	-	-	-	-
Analyse	-	-	-	-
Evaluate	-	-	-	-
Create	-	20	-	-
Total	20	20	10	100

DST - Drill Square Test AM - Aero Modelling SBM - Swachh Bharat Mission

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
Common to ALL Branches								
60 AB 001 - NCC Studies (Air Wing) – I								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

NCC Organisation and National Integration* NCC Organization – History of NCC- NCC Organization – NCC Training – NCC Uniform – Promotion of NCC cadets – Aim and Advantages of NCC Training – NCC Badges of Rank – Honors" and Awards – Incentives for NCC Cadets by Central and State Govt. History and Organization of IAF – Indo-PakWar-1971 – Operation Safed Sagar .National Integration – Unity in diversity – Contribution of Youth in Nation Building-National Integration Council – Images and Slogans on National Integration.	[12]
Drill and Weapon Training* Basic Physical Training – Various Exercises for Fitness (with Demonstration) – Food – Hygiene and Cleanliness. Drill – Words of Commands- Position and Commands– Sizing and Forming – Saluting – Marching – Turning on the march and wheeling – Saluting on the march – Sidepace, Pace forward and to the rear – Marking time – Drill with arms – Ceremonial drill – Guard mounting.(WITH DEMONSTRATION)	[12]
Principles of Flight* Laws of Motion – Forces Acting on Aircraft - Bernoulli"s Theorem - Staling – Primary control surfaces - Secondary control surfaces – Aircraft recognition.	[12]
Aero Engines* Introduction of Aero Engine – Types of Engines – Piston Engine – Jet Engines –Turboprop Engines – Basic Flight Instruments – Modern trends.	[12]
Aero Modeling* History of Aero modelling – Materials used in Aeromodeling – Types of Aeromodels – Static Models – Gliders – Control line models – Radio Control Models-Building and Flying of Aeromodels.	[12]
Total Hours: (Lecture - 30; Practical - 30):	60

Text Book(s):	
1.	"National Cadet Corps- A Concise hand book of NCC Cadets", Ramesh Publishing House, NewDelhi,2014.
Reference(s):	
1.	"Cadets Handbook–Common Subjects SD/SW",published by DGNCC,New Delhi.
2.	"Cadets Handbook-Specialized Subjects SD/SW",published by DGNCC,NewDelhi.
3.	"NCCOTA Precise", published by DGNCC, NewDelhi.

*SDG 4 – Quality Education

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K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Assessment Pattern -Theory					
Test / Bloom's Category*	**Knowledge (K1)%**	**Apply (K2)%**	**Analyzing(K3) %**	**Creating(K4)%**	**Total %**
CAT1	-	-	-	-	-
CAT2	-	-	-	-	-
CAT3	-	-	-	-	-
ESE	The examination and award of marks will be done by the Ministry of Defence, Government of India which includes all K1 to K4 knowledge levels. The maximum marks for the End Semester Examination is 500 marks. It will be converted to100 marks.				

Course Designer(s)

1. Flt Lt V.R.SADASIVAM- sadasivam@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
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60 AB 002	National Cadet Corps- ARMY WING	Category	L	T	P	Credit
		HS	2	0	2	3

Objectives

- Develop character, camaraderie
- Inculcate discipline, secular outlook
- Enrich the spirit of adventure, sportsman spirit
- Ideals of selfless service amongst cadets by working in teams
- Improve qualities such as self-discipline, self-confidence, self-reliance and dignity of labour in the cadets

Pre-requisites

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Display sense of patriotism, secular values and shall be transformed into motivated youth who will carry out nation building through national unity and social cohesion.	Understand
CO2	Demonstrate Health Exercises, the sense of discipline, improve bearing, smartness, turnout, develop the quality of immediate and implicit obedience of orders.	Apply
CO3	Basic knowledge of weapons and their use and handling.	Understand
CO4	Aware about social evils and shall inculcate sense of whistle blowing against such evils and ways to eradicate such evils	Analyse
CO5	Acquaint, expose & provide knowledge about Army/Navy/ Air force and to acquire information about expansion of Armed Forces, service subjects and important battles	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	-	-	-	-	-	1	-	3	-	-	-	-	-	-	3
CO2	-	-	-	-	-	-	-	2	-	-	-	-	-	-	3
CO3	-	-	-	-	-	1	-	3	-	-	-	-	-	-	3
CO4	-	-	-	-	-	-	-	2	-	-	-	-	-	-	3
CO5	-	-	-	-	-	-	-	3	-	-	-	-	-	-	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom''s Category	Continuous Assessment Tests (Marks)		Model Examination (Marks)	End Sem Examination (Marks)
	1	2		
Remember	10	10	20	20
Understand	20	10	20	20
Apply	20	20	20	20
Analyse	10	10	20	20
Evaluate	-	10	20	20
Create	-	-	-	-
Total	60	60	100	100

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Tiruchengode - 637 215

Syllabus

K. S. Rangasamy College of Technology – Autonomous R2022								
Common to all Branches								
60 AB 002 – National Cadet Corps (Army Wing)								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	**T**	**P**		**C**	**CA**	**ES**	**Total**
VII	2	0	2	60	3	50	50	100

NCC Organization & National Integration* NCC Organization – History of NCC - NCC Organization- NCC Training – NCC Uniform – Promotion of NCC cadets – Aim and Advantages of NCC Training- NCC Badges of Rank - Honors' and Awards – Incentives for NCC Cadets by Central and State Govt. National Integration - Unity in Diversity - Contribution of Youth in Nation Building - National Integration Council- Images and Slogans on National Integration	[12]
Basic Physical Training & Drill* Basic Physical Training – various Exercises for Fitness (with Demonstration) – Food – Hygiene and Cleanliness. Drill – Words of Commands - Position and Commands – Sizing and Forming – saluting – Marching- Turning on the March and Wheeling – Saluting on the March - Side Pace, Pace Forward and to the Rear – Marking time – Drill with arms- Ceremonial Drill - Guard Mounting. (WITH DEMONSTRATION).	[16]
Weapon Training* Main Parts of a Rifle – Characteristics of .303 rifle - Characteristics of .22 Rifle – Loading and Unloading – Position and Holding Safety Precautions – Range Procedure- MPI and Elevation – Group and Snap Shooting – Long/Short Range Firing (WITH PRACTICE SESSION) – Characteristics of 5.56mm rifle - Characteristics of 7.62mm SLR- LMG- Carbine Machine Gun – Pistol.	[12]
Social Awareness and Community Development* Aims of Social Service – Various Means and Ways of Social Services – Family Planning – HIV and AIDS – Cancer its Causes and Preventive Measures - NGO and their Activities- Drug Trafficking- Rural Development Programmes – MGNREGA-SGSYJGSY-NSAP –PMGSY– Terrorism and Counter Terrorism – Corruption – Female Foeticide – Dowry – Child Abuse- RTI Act – RTE Act – Protection of Children from Sexual Offences Act – Civic Sense and Responsibility	[12]
Specialized Subject (ARMY)* Basic Structure of Armed Forces - Military History – War Heroes - Battles of Indo-Pak war – ParamVir Chakra – Career in the Defence Forces – Service Tests and Interviews.	[08]
Total Hours:	**60**
Text Book(s):	

1.	National Cadet Corps- A Concise handbook of NCC Cadets by Ramesh Publishing House, New Delhi, 2014.
2.	Cadets Handbook- Specialized Subjects SD/SW published by DG NCC, New Delhi, 2014.
Reference(s):	
1.	"Cadets Handbook – Common Subjects SD/SW" by DG NCC, New Delhi, 2019.
2.	"Cadets Handbook – Specialised Subjects SD/SW" by DG NCC, New Delhi, 2017.

* SDG 4 - Quality Education

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Course Contents and Lecture Schedule

S.No	Topic	No. of Hours
1	**NCC Organization & National Integration**	
1.1	NCC Organization	1
1.2	History of NCC and NCC Organization	1
1.3	NCC Training and NCC Uniform	1
1.4	Promotion of NCC cadet, Aim and advantages of NCC Training	1
1.5	NCC badges of Rank, Honors' and Awards, Incentives for NCC cadets by central and state govt	2
1.6	National Integration, Unity in diversity	1
1.7	Contribution of youth in nation building	2
1.8	National integration council	1
1.9	Images and Slogans on National Integration	2
2	**Basic Physical Training & Drill**	
2.1	Basic physical Training – various exercises for fitness (with Demonstration)-	3
2.2	Food – Hygiene and Cleanliness.	1
2.3	Drill- Words of commands- position and commands- sizing and forming-	3
2.4	saluting- marching- turning on the march and wheeling-	3
2.5	saluting on the march- side pace, pace forward and to the rear- marking time-	3
2.6	Drill with arms- ceremonial drill- guard mounting. (WITH DEMONSTRATION)	3
3	**Weapon Training Main Parts of a Rifle**	
3.1	Characteristics of 0.303 rifle	1
3.2	Characteristics of 0.22 rifle	2
3.3	Loading and unloading, position and holding safety precautions	2
3.4	Range procedure, MPI and Elevation-	2
3.5	Group and Snap shooting Long/Short range firing (WITH PRACTICE SESSION)	3
3.6	Characteristics of 5.56mm rifle	1
3.7	Characteristics of 7.62mm	1
4	**Social Awareness and Community Development**	
4.1	Aims of Social service, Various Means and ways of social services	1
4.2	Family planning, HIV and AIDS	1
4.3	Cancer its causes and preventive measures	1
4.4	NGO and their activities, Drug trafficking	1
4.5	Rural development programmes	1
4.6	MGNREGA, SGSY, JGSY, NSAP, PMGSY	2
4.7	Terrorism and counter terrorism, Corruption	1
4.8	female foeticide, dowry, child abuse	1
4.9	RTI Act, RTE Act	1
4.10	Protection of children from sexual offences act	1
4.11	Civic sense and responsibility	1
5	**Specialized Subject (ARMY)**	
5.1	Basic structure of Armed Forces	1
5.2	Military History, War heroes	1
5.4	battles of Indo - Pak war	1
5.3	Param Vir Chakra,	1
5.5	Career in the Defence forces	2
5.6	Service tests and interviews.	2

Course Designer(s)

1. Mr.E.Chandra Kumar -chandrakumar@ksrct.ac.in

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60 AC 001	Research Skill Development	Category	L	T	P	Credit
		AC	1	0	0	0

Objectives

- To identify research problems, formulate hypotheses, collect data and test hypotheses
- To prepare and submit quality manuscripts and understand peer review process
- To utilize software tools for effective manuscript preparation and visualization of research data
- To familiarize different journal metrics and author-level quality indicators
- To protect creative works, inventions, and branding elements using IPR

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop structured scientific approach to plan and execute research work	Apply
CO2	Understand the journal requirements to publish research findings effectively	Understand
CO3	Apply various software tools during the manuscript preparation	Apply
CO4	Select suitable journals to publish the work using different publication metrics	Analyse
CO5	Apply the appropriate form of IP protection to a specific invention or creation	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2	2	2	2	-	2	2	3	3	3	-	3	3	-	2
CO2	-	-	-	-	-	-	-	3	3	3	-	3	3	-	2
CO3	-	-	-	-	3	-	-	3	3	3	-	3	3	-	2
CO4	-	-	-	-	-	-	-	3	3	-	-	3	3	-	2
CO5	-	-	2	2	-	-	-	3	3	3	-	3	3	-	2
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

One review at end of the semester

Parameters	Weightage (Marks)
Research Problem Identification (Research gap, SDG, Objectives)	10
Literature Review preparation (Clarity, Number and quality of sources)	20
Patent Draft/ Manuscript Preparation (Structure, Content)	20
Use of software tools (Plagiarism, Reference Management, etc.,)	10
Journal Identification (Aim & scope of the journal, journal metrics)	10
Presentation & Viva voce	30
Total	**100**

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Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
60 AC 001 – Research Skill Development								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	1	0	0	15	0	100	-	100

Research - Scientific Approach* Types of Research - Identification and Clarification of the problem – Problem analysis - Formulating hypothesis, Selection of sample and tools of data collection - Testing the hypothesis - Conclusion	[3]
Manuscript Preparation* Structure of a manuscript - Types of manuscript - Graphical abstract - Highlights - Literature Review - Citation - Reference style - Plagiarism – Journal selection - Peer review process	[3]
Research Toolkit* Software Tools for Writing enhancement - Literature review - Reference management - Data analysis and visualization - Drawing - Plagiarism	[3]
Research Publication Metrics* Journal Index: Scopus - Web of Science - SCI - UGC Care - Q Journal; Journal Metrics: Impact Factor, Cite Score; Quality Indicators: h-index - i-10 index - citations	[3]
Intellectual Property Rights* Patents - Industrial Designs - Copyright - Trademarks - Geographical Indications - Trade Secrets	[3]
Total Hours:	**15**

Reference(s):

1.	Kothari, C.R. and Gaurav Garg, “Research Methodology: Methods and Techniques”, New Age International Publishers, 2023
2.	Chawla H S., “Introduction to Intellectual Property Rights”, CBS Publishers and Distributors Private Limited, 2019

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1	**Research - Scientific Approach**	
1.1	Types of Research - Identification and Clarification of the problem – Problem analysis - Formulating hypothesis	2
1.2	Selection of sample and tools of data collection - Testing the hypothesis - Conclusion	1
2	**Manuscript Preparation**	
2.1	Structure of a manuscript - Types of manuscript - Graphical abstract - Highlights	1
2.2	Literature Review	1
2.3	Citation - Reference style – Plagiarism, Journal selection - Peer review process	1
3	**Research Toolkit**	
3.1	Software Tools for Writing enhancement	1
3.2	Literature review, Reference management	1
3.3	Data analysis and visualization – Drawing, Plagiarism	1
4	**Research Publication Metrics**	
4.1	Journal Index: Scopus - Web of Science - SCI - UGC Care - Q Journal;	1
4.2	Journal Metrics: Impact Factor, Cite	1
4.3	ScoreQuality Indicators: h-index - i-10 index - citations	1
5	**Intellectual Property Rights**	
5.1	Patents	1
5.2	Industrial Designs - Copyright	1
5.3	Trademarks - Geographical Indications - Trade Secrets	1

Course Designer

1. Dr.M.Kathirselvam - mkathirselvam@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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K.S.RANGASAMY COLLEGE OF TECHNOLOGY, TIRUCHENGODE - 637215
(An Autonomous Institution affiliated to Anna University)

B.E. / B.Tech. Degree Programme

SCHEME OF EXAMINATIONS
(For the candidates admitted in 2025-2026)

EIGHTH SEMESTER

S.No.	Course Code	Name of the Course	Duration of Internal Exam (Hrs)	Weightage of Marks			Minimum Marks for Pass in End Semester Exam	
				Continuous Assessment *	End Semester Exam **	Max. Marks	End Semester Exam	Total
THEORY								
1.	60 EV E5*	Professional Elective V	2	40	60	100	45	100
PRACTICAL								
2.	60 EV 8P1	Project Work Phase - II	3	60	40	100	45	100
3.	60 CG 0P6	Internship	-	100	-	100	-	100

* CA evaluation pattern will differ from course to course and for different tests. This will have to be declared in advance to students. The department will put a process in place to ensure that the actual test paper follow the declared pattern.

** End Semester Examination will be conducted for maximum marks of 100 and subsequently be reduced to 60 marks for theory End Semester Examination and 40 marks for practical End Semester Examination.

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60 EV 8P1	Project work Phase - II	Category	L	T	P	Credit
		CG	0	0	16	8

Objectives

- To help the students apply their academic knowledge and technical skills in a specific domain
- Foster collaborative learning skills
- Habituated to critical thinking and use problem solving skills
- Develop self-directed inquiry and life-long skills
- To enhance the communication skills of the students by providing opportunities to discuss in groups and to present their observations, findings and report in formal reviews both in oral and written format

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Identify engineering problems in their domain of interest and carry out literature review in the chosen technical area	Understand
CO2	Analyse and identify an appropriate technique to solve the problem.	Analyse
CO3	Design engineering solution, do experimentation / simulation / programming / fabrication/ collect and interpret data utilizing a systems approach	Analyse
CO4	Communicate effectively in oral and written forms	Apply
CO5	Demonstrate the knowledge, skills and attitudes of a professional engineer as an individual and member of a team	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO2	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO4	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
CO5	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Internal Assessment (60)					End Semester (40)
Items	Review 1	Review 2	Review 3	Publication*	
Marks	5	10	15	30	40
	Total internal marks 60				

Note:

***Publication marks shall be awarded based on the following criteria**

1. SCI / WoS Journal = 30 Marks
2. Scopus Indexed Journal / Scopus Indexed Book Chapters/ IEEE Conference = 27 Marks
3. Journals listed in UGC Care = 25 Marks

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K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV 8P1 - Project work Phase - II								
Semester	**Hours/Week**			**Total Hrs**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	0	0	16	240	8	60	40	100

1. A committee is constituted with the project coordinator, project guide and HOD/Senior professor in the department.
2. Three reviews have to be conducted by the committee
3. Each review has to be evaluated for 100 marks.
4. Attendance is compulsory for all reviews. If a student fails to attend review for some valid reason, one or more chance may be given.
5. A senior professor from other departments may be included in the committee for final review.
6. The report should be submitted as per the format by the students.

*SDG 4 – Quality Education

Course Designer(s)

1. Dr.P.Kumar-kumar@ksrct.ac.in

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60 EV E11	Solid state Electronic Devices	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the fabrication of p-n Junctions.
- To learn the key characteristics and effects of MOS transistor.
- To study the concepts and characteristics of the advanced MOSFET and Integrated circuits.
- To understand the characteristics of the semiconductor microwave and power devices.
- To learn the concepts and applications of various optoelectronic devices.

Pre-requisite

- Electronic Devices

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Illustrate the process of the fabrication of p-n Junctions	Understand
CO2	Describe the characteristics and effects of the MOS transistor.	Understand
CO3	Discuss the advanced MOSFET and Integrated circuits.	Understand
CO4	Examine the characteristics of the semiconductor microwave and power devices.	Understand
CO5	Describe the concepts with applications of various optoelectronic devices.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	2	3	2	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	2	2	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	2	-	-	-	-	-	-	-	-	2	2	-
CO4	3	3	3	2	2	-	-	-	-	-	-	-	3	3	-
CO5	3	2	3	2	3	-	-	-	-	-	-	-	3	2	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	30
Understand	40	40	70
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV E11- Solid state Electronic Devices								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

Fabrication Fabrication of PN junction: Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion Implantation, Chemical Vapour Deposition, Photolithography, Etching, Metallization - Equilibrium Conditions - Forward- and Reverse - Biased Junctions, Steady State Conditions.	[9]
MOS Transistors MOS Inverter Circuits - Threshold Voltage and the Body Effect, Current/voltage Characteristics, Subthreshold Current, Short Channel Effect and Narrow Width Effect, Drain Induced Barrier Lowering Channel Length Modulation, Hot Carrier Effects, Effective Mobility and Velocity Saturation SPICE Models.	[9]
Advanced MOSFET and Integrated Circuits Metal Gate-High-k - Enhanced Channel Mobility Materials and Strained Si FETs - SOI MOSFETs and FinFETs - Monolithic Device Elements - Charge Transfer Devices, Applications of CCDs - Ultra Large Scale Integration (ULSI).	[9]
Semiconductor Microwave and Power Devices Tunnel Diodes – IMPATT - TRAPATT Diode - Gunn Diode, Electron Mechanism, Formation and Drift of Space Charge Domains - P-N-P-N Diode - Semiconductor Controlled Rectifier - Power Semiconductor Devices: Construction, Principle of Operation, Characteristics and Applications of SCR, LASCR, DIAC, TRIAC, GTO Thyristors - Power MOSFET - DMOS - VMOS.	[9]
Opto-Electronic Devices* Optical Absorption - Photo-Detector - Spin LEDs and LCDs - Laser, Semiconductor Lasers, Photoconductor - Photodiode, Phototransistor - Solar cell - PIN photodiode, Charge-Coupled Devices, APD and Its Applications.	[9]
Total Hours :	**45**

Text Book(s):	
1.	Ben G. Streetman and Sanjay Banerjee, “Solid State Electronic Devices”, 7th Edition, Pearson Education, 2015.
2.	David A. Bell, “Electronic Devices and Circuits”, 5th Edition, Oxford University press, 2017.
Reference(s):	
1.	Pallab Bhattacharya “Semiconductor Opto Electronic Devices”, Prentice Hall of India Pvt., Ltd., New Delhi, 2nd Edition, 2017.
2.	Jacob Millman, Christos Halkias, Chetan D Parikh, “Integrated Electronics: Analog and Digital Circuits and Systems”, 2nd Edition, Tata Mcgraw Hill Education Private Limited, 2011.
3.	Sze S.M., KwokK. Ng," Physics of Semiconductor Devices", 3rd Edition, Wiley, 2018.
4.	Arora N.D., “MOSFET Models for VLSI Circuit Simulation Theory and Practice”, Springer, 2012.

*SDG: 9 - Industry, Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Fabrication**	
1.1	Fabrication of PN junction: Thermal Oxidation	1
1.2	Diffusion, Rapid Thermal Processing	1
1.3	Ion Implantation	1
1.4	Chemical Vapour Deposition	1
1.5	Photolithography, Etching	1
1.6	Metallization	1
1.7	Equilibrium Conditions	1
1.8	Forward- and Reverse - Biased Junctions	1
1.9	Steady State Conditions	1
2	**MOS Transistors**	
2.1	MOS Inverter Circuits	1
2.2	Threshold Voltage and the Body Effect	1
2.3	Current/voltage Characteristics	1
2.4	Subthreshold Current	1
2.5	Short Channel Effect	1
2.6	Narrow Width Effect, Drain Induced Barrier Lowering Channel Length Modulation	1
2.7	Hot Carrier Effects	1
2.8	Effective Mobility	1
2.9	Velocity Saturation SPICE Models.	1
3	**Advanced MOSFET and Integrated Circuits**	
3.1	Metal Gate-High-k	1
3.2	Enhanced Channel Mobility Materials	1
3.3	Strained Si FETs	1
3.4	SOI MOSFETs	1
3.5	FinFETs	1
3.6	Monolithic Device Elements	1
3.7	Charge Transfer Devices	1
3.8	Applications of CCDs	1
3.9	Ultra Large Scale Integration (ULSI)	1
4	**Semiconductor Microwave and Power Devices**	
4.1	Tunnel Diodes – IMPATT	1
4.2	TRAPATT Diode - Gunn Diode	1
4.3	Electron Mechanism, Formation and Drift of Space Charge Domains	1
4.4	P-N-P-N Diode - Semiconductor Controlled Rectifier	1
4.5	Power Semiconductor Devices: Construction	1
4.6	Principle of Operation, Characteristics	1
4.7	Applications of SCR, LASCR, DIAC	1
4.8	TRIAC, GTO Thyristors	1
4.9	Power MOSFET - DMOS - VMOS	1
5	**Opto-Electronic Devices**	
5.1	Optical Absorption	1
5.2	Photo-Detector - Spin LEDs	1
5.3	LCDs - Laser	1
5.4	Semiconductor Lasers	1
5.5	Photoconductor - Photodiode	1
5.6	Phototransistor - Solar cell	1
5.7	PIN photodiode	1
5.8	Charge-Coupled Devices	1
5.9	APD and Its Applications	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV E12	Analog VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To describe the fabrication process, layout considerations and design rules for BiCMOS technology
- To analyse and improve the performance of inverting amplifiers using MOS and bjt technologies
- To identify different noise sources in analog and their representation
- To explain the principles of ideal analog – to - digital (A/D) and digital – to - analog (D/A) converters.
- To apply fault modelling and simulation techniques for analog VLSI circuits

Pre-requisites

- Digital Design

Course Outcomes

On The Successful Completion of the Course, Students Will Be able To

CO1	Recall basic MOS device models and their parameters.	Remember
CO2	Interpret the behaviour of current sources, sinks, and mirrors.	Understand
CO3	Identify and differentiate between various noise sources (thermal, flicker) in analog circuits.	Analyse
CO4	Identify and quantify quantization noise in a/d and d/a conversion	Apply
CO5	Describe fault modelling and simulation techniques for analog VLSI circuits.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO2	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO3	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO4	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO5	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	34
Understand	40	25	66
Apply	-	-	-
Analyse	-	15	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV E12- Analog VLSI Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

Analog Circuits and Amplifiers* Voltage and Current References, Comparator, Multiplier, Amplifiers - MOS and BJT Inverting Amplifier - Improving Performance of Inverting Amplifier - CMOS and BJT Differential Amplifiers	[9]
Operational Amplifiers* Characterization of Op - Amp - The BJT Two Stage Op - amp - The CMOS Two Stage Op - Amp, Op - Amps with Output Stage, Folded Cascode Op - Amp, Transconductance Amplifier - Instrumentation Amplifier.	[9]
Noise and Filters* Noise Spectrum, Sources, Types, Thermal and Flicker Noise, Representation in Circuits, Noise Bandwidth, Noise Figure. Low pass filters - High Pass Filters – Band Pass Filters – Switched Capacitor Filters - Phase Locked Loops.	[9]
D/A and A/D Converters* Ideal A/D and D/A Converters, Quantization Noise, Signed Codes, Performance Limitations. D/A converter: Current scaling, Voltage Scaling and Charge Scaling D/A Converters - Serial D/A Converters - Serial A/D Converters, Parallel - High Performance A/D Converters.	[9]
Analog VLSI Testing and Systems * FAULT Modelling and Simulation - BIST – Analog VLSI for Vision - System Design Issues - An Integrated Image Acquisition, Smoothing and Segmentation Focal Plane Processor	[9]
Total Hours:	**45**

Text Book(s):	
1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2nd Edition 2002. 2018.
2.	Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., “Analysis and Design of Analog Integrated Circuits”, John Wiley, 5th Edition, 2001.
Reference(s):	
1.	Mohammed Ismail, “Analog VLSI signal and Information processing”, McGraw-Hill, 1994.
2.	John L. Wyatt et.al, “Analog VLSI Systems for Image Acquisition and Fast Early Vision Processing”, International Journal of Computer Vision
3.	Douglas R. Holberg Phillip E. Allen, “CMOS Analog Circuit Design”, Oxford University Press, 2nd Edition, 2012.
4.	Jacob Baker R, “CMOS Circuit Design, Layout and Simulation”, 2010, 3rd Edition, IEEE Press Series on Microelectronic Systems, Wiley Publications.

*SDG: 4 - Quality Education

Course Contents and Lecture Schedule

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Tiruchengode - 637 215

S. No.	Topics	No. of hours
1.0	**Basic Mos Device Physics**	
1.1	Voltage and Current References	1
1.2	Comparator	1
1.3	Multiplier	1
1.4	BJT Amplifier	1
1.5	MOS Amplifier	1
1.6	Improving Performance of Inverting Amplifier	1
1.7	BJT Differential Amplifiers	2
1.8	CMOS Differential Amplifiers	1
2.0	**Basic Analog Circuits and Amplifiers**	
2.1	Design and Analysis of Current Sources and Sinks (Simple, Cascode, Wilson Current Mirrors).	1
2.2	Introduction to Voltage and Current References (Bandgap References).	1
2.3	Design of Comparators (Open - Loop, Closed - Loop).	1
2.4	Introduction to Analog Multipliers (Gilbert Cell).	2
2.5	Design of MOS and BJT Inverting Amplifiers (Frequency Response, Gain).	1
2.6	Techniques for Improving the Performance of Inverting Amplifiers (Cascoding, Miller Effect Compensation).	1
2.7	Design of CMOS and BJT Differential Amplifiers (Common - Mode Rejection Ratio (CMRR), Differential Gain).	1
2.8	Characterization of Operational Amplifiers (Op - Amps) (Gain, Bandwidth, Slew Rate, Input/Output Impedance).	1
3.0	**Noise and Filters**	
3.1	Introduction to Noise in Analog Circuits (Thermal Noise, Flicker Noise).	1
3.2	Noise Sources in MOS and BJT Transistors (Shot Noise).	1
3.3	Representing Noise in Circuits (Noise Spectral Density, Noise Bandwidth).	1
3.4	Calculation of Noise Figure in Analog Circuits	1
3.5	Design of Low - Pass Filters (Passive and Active Filters, First - Order and Higher - Order Filters).	1
3.6	Design of High - Pass Filters (Passive and Active Filters).	1
3.7	Design of Band - Pass Filters (Active Filters).	1
3.8	Introduction to Switched Capacitor Filters (Basic Building Blocks, Applications).	1
3.9	Introduction to Phase - Locked Loops (PLLs) (Basic Operation, Applications).	1
4.0	**D/A and A/D Converters**	
4.1	Introduction to Ideal A/D and D/A Converters (quantization process).	1
4.2	Quantization Noise in A/D and D/A Converters	1
4.3	Introduction to Signed Binary Codes (Two's Complement, Offset Binary).	1
4.4	Performance Limitations of A/D and d/a Converters (Resolution, Accuracy, Speed).	1
4.5	Design of Current Scaling D/A Converters (Single - Bit and Multi - Bit)	1
4.6	Design of Voltage Scaling D/A Converters (Single - Bit and Multi - Bit).	1
4.7	Design of Charge Scaling D/A Converters	1
4.8	Design of Serial and Parallel D/A Converters.	2
4.9	Introduction to High - Performance A/D Converters (Flash Converters, Pipeline Converters).	1
5.0	**Analog VLSI Testing and Systems**	
5.1	Fault Modeling and Simulation Techniques for Analog Circuits	1
5.2	Built-In Self - Test (BIST) for Analog Circuits.	1
5.3	Applications of Analog VLSI for Vision Systems (Image Sensors, Analog Signal Processing).	1
5.4	Design Considerations for Analog VLSI Systems (Power Dissipation, Noise).	2
5.5	Segmentation Focal Plane Processor	1
5.6	Case study: An integrated Image Acquisition	2
5.7	Case study: Smoothing	1

Course Designer(s)

1. Saravanan S – saravanan.s@ksrct.ac.in

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60 EV E13	ASIC Synthesis and STA	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the ASIC design methodology, including pre-layout and post-layout steps.
- To develop synthesizable RTL using logic inference, partitioning, and design constraints.
- To define and apply timing constraints for effective RTL synthesis and clock management.
- To explore optimization techniques for performance, power, and area during synthesis.
- To perform static timing analysis for verifying timing correctness and identifying critical paths.

Pre-requisites

- Digital Design, Electronics Fundamental and CMOS Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the complete ASIC design flow, including logic libraries and layout stages.	Understand
CO2	Develop synthesizable RTL code and apply design partitioning and logic inference techniques.	Understand
CO3	Define timing constraints and address clocking issues to ensure synthesis quality.	Understand
CO4	Apply performance, power, and area optimization strategies during RTL compilation.	Understand
CO5	Perform static timing analysis and identify critical paths and timing violations in ASIC designs.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-	3	3	-
CO5	3	3	-	-	3	-	-	3	3	-	3	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	10
Understand	40	40	70
Apply	10	10	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E13 - ASIC Synthesis and STA

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

ASIC Design & Synthesis ASIC design methodology- Pre-Layout Steps- Post-Layout Steps- Logic Library.	[9]
Synthesizable RTL Introduction of RTL -Partitioning for Synthesis- Logic Inference- Constraining designs.	[9]
Timing Constraint Development Environment and Constraints- Advanced Constraints- Clocking Issues-Pre-Synthesis checks- RTL Synthesis.	[9]
Performance Optimization Design Space Exploration-Total Negative Slack- Compilation Strategies- Optimization Techniques- Power Optimization- Area Optimization.	[9]
Static Timing Analysis* STA Concepts-Types of Paths- Pre-Layout Timing Analysis & checks-Setup Timing Check. Hands on: Design and Synthesis of UART	[9]
Total Hours:	**45**

Text Book(s):

1.	Himanshu Bhatnagar, “Advanced ASIC Chip Synthesis”, Kluwer Academic Publishers, Second Edition, 2002.
2.	Bhasker J. & Rakesh Chadha, “Static Timing Analysis for Nano meter Designs A Practical Approach”, Springer, 2009.

Reference(s):

1.	Khosrow Golshan, “Physical Design Essentials - An ASIC Design Implementation Perspective”, Springer, 2007.
2.	Veena S. Chakravarthi, Shivananda R. Koteshwar,”SoC Physical Design - A Comprehensive Guide”, Springer, 2022.
3.	Design Compiler ® User Guide, Synopsys, 2016.
4.	Ahsan Kazmi S. M., Latif U. Khan, Choong Seon Hong, Nguyen H. Tran, “Network Slicing for 5G and Beyond Networks”, Springer International Publishing, 2020.

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**ASIC Design & Synthesis**	
1.1	ASIC design methodology	2
1.2	Pre-Layout Steps	3
1.3	Post-Layout Steps	2
1.4	Logic Library.	2
2.0	**Synthesizable RTL**	
2.1	Introduction of RTL	1
2.2	Partitioning for Synthesis	2
2.3	Logic Inference	3
2.4	Constraining designs	3
3.0	**Timing Constraint Development**	
3.1	Environment and Constraints	2
3.2	Advanced Constraints	1
3.3	Clocking Issues	2
3.4	Pre-Synthesis checks	2
3.5	RTL Synthesis	2
4.0	**Performance Optimization**	
4.1	Design Space Exploration	1
4.2	Total Negative Slack	2
4.3	Compilation Strategies	2
4.4	Optimization Techniques	2
4.5	Area Optimization	2
5.0	**Static Timing Analysis**	
5.1	STA Concepts	1
5.2	Types of Paths	2
5.3	Pre-Layout Timing Analysis	2
5.4	Checks-Setup Timing Check	2
5.5	Hands on: Design and Synthesis of UART	2

Course Designer(s)

1. Mrs.C.Saranya - saranyac@ksrct.ac.in

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Chairman - Board of Studies
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60 EV E14	HDL Programming	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To know the basic language features of verilog HDL, VHDL and the role of HDL in CMOS circuits
- To understand the dataflow, gate level and behavioural modelling in HDL
- To study about various combinational circuits using verilog HDL
- To learn the theoretical aspects of system verilog HDL
- To learn the fundamental principles of test bench and design in verilog HDL and its applications

Pre-requisites

- Digital Logic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply digital design concepts and write verilog programs in gate level and transistor level modelling	Apply
CO2	Describe the types of modelling in verilog HDL	Understand
CO3	Design and develop the combinational circuits using verilog HDL modelling	Apply
CO4	Design and develop the sequential circuits using verilog HDL modelling	Apply
CO5	Analyse the process of synthesizing the digital system and interface test bench environment	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	3	3	-	-	-	-	-	3	3	-
CO4	3	3	3	3	3	3	3	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	3	3	-	-	-	-	-	3	3	-
3 - Strong; 2 - Medium; 1 – Some-															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	-	10
Understand	30	30	60
Apply	20	30	20
Analyse	-	-	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E – Electronics Engineering (VLSI Design & Technology)

60 EV E14 - HDL Programming

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

HDL* Digital Design Using Verilog HDL And VHDL, Typical HDL Design Flow -Hierarchical Modelling Concepts - Verilog Operators and Modules - Verilog Ports, Data Types and Assignments - Levels In Verilog HDL: Gate Level - Data Flow Level and Behaviour Level, Switch Level Modelling - Modelling of CMOS Gates and Boolean Functions, Tasks and Functions	[9]
Dataflow, Gate Level and Behavioural Modelling* Dataflow Modelling and Behavioural Modelling - Gate Types, Gate Primitive, Data Types, Concurrent Statement - Sequential Assignment Statements - Structured Procedures, Process Statement, Propagation Delay and Continuous Assignments	[9]
Combinational Circuit using Verilog HDL* HDL Design: Arithmetic Logic Unit - Binary Adder/Subtractor, Full Adder - Full Subtractor - Half-Adder - Half-Subtractor – Priority Encoder, Encoders, Decoders - Multiplexer, Demultiplexers, Comparator – Parity Checker, Code Converters	[9]
Sequential Circuit using Verilog HDL* Combinational Versus Sequential Logic - Classification of Sequential Logic - HDL Design: Latch, Flip-Flops – Synchronous Counters - Shift Counters - Shift Registers - Finite State Machine In HDL	[9]
Verilog HDL Synthesis & Test bench* Synthesis Design Flow - Verification of the Gate Level Net List - Modelling For Logic Synthesis - Example of Combinational Logic, Sequential Circuit With Latches, Flip - Flops Synthesis - FIR Filter Using Verilog HDL. Writing Test Benches In Verilog HDL - Separating the Test Bench and Design - The Interface Construct - Stimulus Timing. **Hands On:** 1. Write A Verilog Program For The Combinational Design Along With a Test Bench to Verify The Design. 2. Simulation of Verilog HDL Code For Sequential Logic Circuits.	[9]
Total Hours:	**45**

Text Book(s):

1.	Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education New Delhi, 2019.
2.	Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, 2nd Edition, Springer, 2012.

Reference(s):

1.	https://ocw.mit.edu – Massachusetts Institute of Technology Open Courseware.
2.	Donald Thomas, “Logic Design and Verification Using System Verilog”, Create Space Independent Publishing Platform, 2014
3.	Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2nd Edition, PHI, 2009.
4.	Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**HDL**	
1.1	Digital Design Using Verilog HDL And VHDL	1
1.2	Typical HDL Design Flow	1
1.3	Hierarchical Modelling Concepts	1
1.4	Verilog Operators and Modules	1
1.5	Verilog Ports, Data Types and Assignments	1
1.6	Levels In Verilog HDL: Gate Level - Data Flow Level	1
1.7	Behaviour Level, Switch Level Modelling	1
1.8	Modelling of CMOS Gates and Boolean Functions	1
1.9	Tasks and Functions	1
2.0	**Dataflow, Gate Level and Behavioural Modelling**	
2.1	Dataflow Modelling	2
2.2	Behavioural Modelling	2
2.3	Gate Types, Gate Primitive, Data Types	1
2.4	Concurrent Statement - Sequential Assignment Statements	1
2.5	Structured Procedures, Process Statement	1
2.6	Propagation Delay and Continuous Assignments	2
3.0	**Combinational Circuit using Verilog HDL**	
3.1	Arithmetic Logic Unit	1
3.2	Binary Adder/Subtractor	1
3.3	Full Adder - Full Subtractor	1
3.4	Half-Adder - Half-Subtractor	2
3.5	Priority Encoder, Encoders, Decoders	1
3.6	Multiplexer, Demultiplexers	1
3.7	Comparator – Parity Checker	1
3.8	Code Converters	1
4.0	**Sequential Circuit using Verilog HDL**	
4.1	Combinational Versus Sequential Logic	1
4.2	Classification of Sequential Logic	2
4.3	HDL Design: Latch, Flip-Flops	2
4.4	Synchronous Counters - Shift Counters	2
4.5	Shift Registers	1
4.6	Finite State Machine In HDL	1
5.0	**Verilog HDL Synthesis & Test bench**	
5.1	Synthesis Design Flow	1
5.2	Verification of the Gate Level Net List	1
5.3	Modelling For Logic Synthesis	1
5.4	Example of Combinational Logic, Sequential Circuit With Latches, Flip - Flops	1
5.5	FIR Filter Using Verilog HDL	1
5.6	Writing Test Benches In Verilog HDL	1
5.7	Separating the Test Bench and Design	1
5.8	The Interface Construct	1
5.9	Stimulus Timing	1

Course Designer(s)

1. Mr.D.Poornakumar – poornakumard@ksrct.ac.in

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60 EV E15/60 EV L02	FPGA Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the architecture of FPGA systems
- To learn the fundamental principles and components of FPGA fabrics
- To analyse the design of combinational logic using FPGA
- To analyse the design of sequential logic using FPGA
- To explain the large scale FPGA system architecture

Pre-requisites

- Digital system design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the different FPGA architecture for digital system design.	Understand
CO2	Interpret the components used for FPGA fabrics	Understand
CO3	Analyse the parameters of combinational logic digital system.	Analyse
CO4	Analyse the parameters of sequential logic digital system.	Analyse
CO5	Illustrate the large scale FPGA system architecture.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	-	-	-	-	-	-	-	-	3	3	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	40	60
Apply	-	-	-
Analyse	-	10	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV E15/60 EV L02 - FPGA Design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

FPGA Based Systems* Digital Design and FPGA's - FPGA Based System Design - Problems in VLSI Technology behind FPGA/CPLD - Manufacturing Processes - CMOS Logic Gates - Wires, Registers and RAM - Packages and Pads, Digital Clock Manager (DCM).	[9]
FPGA Fabrics* FPGA Fabrics - FPGA Architectures - SRAM Based FPGAs, Permanently Programmed FPGAs - Chip I/O Circuit Design of FPGA Fabrics - Architecture of FPGA Fabrics. Application and Implementation of Digital Design in FPGA - Programming, Synthesis, FPGA Integration, Place and route.	[9]
Combinational Logic* Combinational Logic - The Logic Design Process-Hardware Description Languages - Combinational Network Delay - Power and Energy Optimization - Arithmetic Logic - Logic Implementation of FPGAs - Physical Design of FPGAs.	[9]
Sequential Machines* Sequential Machines - The Sequential Machine Design Process - Sequential Design Styles - Rules for Clocking - Performance Analysis - Power Optimization.	[9]
Large Scale Systems* Design Methodologies - Design Example - Large Scale Systems-Busses - Platform FPGAs - Multi FPGA Systems.	[9]
Total Hours:	**45**

Text Book(s):	
1.	Wayne Wolf, "FPGA – Based System Design", Prentice Hall of India Private Ltd., 2013.
2.	Wayne Wolf, "Modern VLSI Design: System-on-Chip Design", 3rd Edition, Prentice Hall of India Private Ltd., 2012.
Reference(s):	
1.	Trimberger S., "Field Programmable Gate Array Technology", Springer US, 2012.
2.	John V.Oldfield, Richard C Dorf, "Field Programmable Gate Arrays", John Wiley & Sons, 2013.
3.	Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2011.
4.	Wayne Wolf, "FPGA Based System Design Hardcover – Import", PTR Prentice Hall Englewood, 2004.

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**FPGA Based Systems**	
1.1	Digital Design and FPGA's	1
1.2	FPGA Based System Design	2
1.3	Problems in VLSI Technology behind FPGA/CPLD	1
1.4	Manufacturing Processes - CMOS Logic Gates-Wires, Registers and RAM	2
1.5	Packages and Pads	1
1.6	Digital Clock Manager (DCM).	2
2.0	**FPGA Fabrics**	
2.1	FPGA Fabrics	1
2.2	FPGA Architectures - SRAM Based FPGAs	2
2.3	Permanently Programmed FPGAs	1
2.4	Chip I/O Circuit Design of FPGA Fabrics	1
2.5	Architecture of FPGA Fabrics	1
2.6	Application and Implementation of Digital Design in FPGA - Programming, Synthesis	1
2.7	FPGA Integration	1
2.8	Place and route	1
3.0	**Combinational Logic**	
3.1	Combinational Logic	1
3.2	The Logic Design Process	1
3.3	Hardware Description Languages	1
3.4	Combinational Network Delay	2
3.5	Power and Energy Optimization	1
3.6	Arithmetic Logic	1
3.7	Logic Implementation of FPGAs	1
3.8	Physical Design of FPGAs.	1
4.0	**Sequential Machines**	
4.1	Sequential Machines	1
4.2	The Sequential Machine Design Process	2
4.3	Sequential Design Styles	1
4.4	Rules for Clocking	1
4.5	Performance Analysis	2
4.6	Power Optimization	2
5.0	**Large Scale Systems**	
5.1	Design Methodologies	2
5.2	Design Example	1
5.3	Large Scale Systems	1
5.4	Busses	2
5.5	Platform FPGAs	1
5.6	Multi FPGA Systems	2

Course Designer(s)

1. Mr.D. Poornakumar – poornakumard@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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60 EV E16	Data Science	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the data science fundamentals and process
- To learn to describe the data for the data science process
- To learn to describe the relationship between data
- To utilize the python libraries for data wrangling
- To present and interpret data using visualization libraries in python

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the data science process	Understand
CO2	Use the different types of data description for data science process	Apply
CO3	Illustrate the relationships between data	Apply
CO4	Use the Python Libraries for Data Wrangling	Apply
CO5	Apply visualization Libraries in Python to interpret and explore data	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	-	-	-	-	3	3	3	-	-	3	2	3
CO2	3	3	3	-	3	-	-	3	3	3	-	3	3	2	3
CO3	3	3	2	-	3	-	-	3	3	3	-	-	3	2	3
CO4	3	3	3	-	3	-	-	3	3	3	-	3	3	2	3
CO5	3	3	3	-	3	-	-	3	3	3	-	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	10	10
Understand	20	20	40
Apply	10	30	50
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E16 - Data Science

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
V	3	0	0	45	3	40	60	100

Data Science Process* Data Science: Benefits and Uses – Facets of Data - Data Science Process: Defining Research Goals – Retrieving Data – Data Preparation - Exploratory Data Analysis – Build The Model – Presenting Findings and Building Applications - Data Mining - Data Warehousing – Basic Statistical Descriptions of Data.	[9]
Describing Data* Types of Data - Types of Variables -Describing Data With Tables and Graphs – Describing Data With Averages - Describing Variability - Normal Distributions and Standard (Z) Scores. **Hands-On:** Install the Data Analysis And Visualization Tool: R/ Python /Tableau Public/ Power BI	[9]
Describing Relationships* Correlation –Scatter Plots –Correlation Coefficient for Quantitative Data –Computational Formula for Correlation Coefficient – Regression –Regression Line –Least Squares Regression Line – Standard Error of Estimate – Interpretation of R2 –Multiple Regression Equations –Regression Towards The Mean.	[9]
Python Libraries for Data Wrangling ** ** Numpy Arrays –Aggregations –Computations on Arrays –Comparisons, Masks, Boolean Logic – Fancy Indexing – Structured Arrays – Data Manipulation With Pandas – Data Indexing And Selection – Operating on Data – Missing Data – Hierarchical Indexing – Combining Datasets – Aggregation And Grouping – Pivot Tables. **Hands-On: • Perform Exploratory Data Analysis (EDA) on With Datasets Like Email Data Set. Export All Your Emails as A Dataset, Import Them Inside a Pandas Data Frame, Visualize Them and Get Different Insights from the Data.	[9]
Data Visualization** Importing Matplotlib – Line Plots – Scatter Plots – Visualizing Errors – Density And Contour Plots – Histograms – Legends – Colors – Subplots – Text And Annotation – Customization – Three-Dimensional Plotting - Geographic Data With Basemap - Visualization With Seaborn. **Hands-On:** • Working With Numpy Arrays, Pandas Data Frames, Basic Plots Using Matplotlib. Perform Eda On Wine Quality Data Set • Use A Case Study On A Data Set and Apply The Various EDA and Visualization Techniques and Present an Analysis Report. • Perform Time Series Analysis and Apply the Various Visualization Techniques.	[9]
Total Hours:	**45**

Text Book(s):	
1.	David Cielen, Arno D. B. Meysman, and Mohamed Ali, “Introducing Data Science”, Manning Publications, 2016. (Unit I)
2.	Robert S. Witte and John S. Witte, “Statistics”, 11th Edition, Wiley Publications, 2017. (Units II and III)
Reference(s):	
1.	Jake VanderPlas, “Python Data Science Handbook”, O’Reilly, 2016. (Units IV and V)
2.	Allen B. Downey, “Think Stats: Exploratory Data Analysis in Python”, Green Tea Press,2014
3.	Eric Pimpler, “Data Visualization and Exploration with R”, Geospatial Training service, 2017.
4.	Suresh Kumar Mukhiya, Usman Ahmed, “Hands-On Exploratory Data Analysis with Python”, Packt Publishing, 2020.

***SDG: 4 - Quality Education**

****SDG: 9 - Industry Innovation and Infrastructure**

Passed in BoS Meeting held on 13/06/2025

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Data Science Process**	
1.1	Data Science: Benefits and Uses, Facets of Data	1
1.2	Data Science Process: Overview	1
1.3	Defining Research Goals, Retrieving Data, Data Preparation	1
1.4	Exploratory Data Analysis, Build The Model, Presenting Findings and Building Applications	1
1.5	Data Mining, Data Warehousing	1
1.6	Basic Statistical Descriptions of Data	1
2.0	**Describing Data**	
2.1	Types of Data, Types of Variables	1
2.2	Describing Data With Tables and Graphs	1
2.3	Describing Data With Averages	1
2.4	Describing Variability	1
2.5	Normal Distributions and Standard (Z) Scores	2
2.6	Hands On	2
3.0	**Describing Relationships**	
3.1	Correlation, Scatter Plots	1
3.2	Correlation Coefficient for Quantitative Data	1
3.3	Computational Formula for Correlation Coefficient	1
3.4	Regression, Regression Line, Least Squares Regression Line	1
3.5	Standard Error of Estimate, Interpretation of R2	1
3.6	Multiple Regression Equations, Regression Towards the Mean	1
4.0	**Python Libraries For Data Wrangling**	
4.1	Numpy Arrays, Aggregations	1
4.2	Computations on Arrays, Comparisons	1
4.3	Masks, Boolean Logic, Fancy Indexing	1
4.4	Structured Arrays, Data Manipulation With Pandas	1
4.5	Data Indexing and Selection, Operating on Data, Missing Data	1
4.6	Hierarchical Indexing, Combining Datasets, Aggregation and Grouping, Pivot Tables	1
4.7	Hands on	4
5.0	**Data Visualization**	
5.1	Importing Matplotlib, Line Plots, Scatter Plots	1
5.2	Visualizing Errors, Density and Contour Plots	1
5.3	Histograms, Legends, Colors	1
5.4	Subplots, Text and Annotation	1
5.5	Customization, Three-Dimensional Plotting	1
5.6	Geographic Data With Basemap, Visualization With Seaborn	1
5.7	Hands On	9
	Total	45

Course Designer(s)

1. Mrs.K.Vanitha – vanitha@ksrct.ac.in

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60 EV E21	Semiconductor Equipment Design and Technology	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand pressure regimes, gas behavior, vacuum pumps and gauges, system design considerations and leak detection
- To explore plasma physics, particle motion in electric and magnetic fields, plasma response to various fields and plasma potential
- To learn about chamber pump systems, load locks, mass flow control, hazardous gas handling and various pressure gauges
- To understand RF and microwave power sources, coupling techniques, capacitively and inductively coupled plasmas and ion bombardment processes
- To explore how vacuum and plasma technologies are utilized in etching, deposition, sputtering and ashing processes

Pre-requisites

- Electronic Devices

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the operation of different types of vacuum pumps (diaphragm, blowers, diffusion, cryogenic, turbo molecular)	Understand
CO2	Explain the motion of charged particles in electric and magnetic fields	Understand
CO3	Illustrate the effectiveness of different pumping systems for plasma reactors	Understand
CO4	Describe the principles of RF and microwave coupling in plasma systems	Understand
CO5	Interpret the suitability of different thin - film processing techniques (sputtering, deposition, etching, ashing) for specific applications	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO2	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO3	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO4	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
CO5	3	3	3	3	-	-	3	-	-	-	-	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	30
Understand	40	40	70
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV E21- Semiconductor Equipment Design and Technology								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Fundamentals of Vacuum Technology* Vacuum Nomenclature, Gas Properties, Molecular Processes And Kinetic Theory, Throughput, Pumping Speed, Gas Flow – Flow Calculations, Technology of Vacuum Pumps - Diaphragm Pumps, Vacuum Blowers, Diffusion Pumps, Cryogenic Pumps, Pumps For Ultra-High Vacuum, Vacuum Measurements, Types of Gauges, Mass Analysis And Spectrometry, Mass Flow Control And Measurement, Vacuum Valves, Flanges And Components, Viewports, Outgassing of Materials, High – Vacuum - Based Processes: Sputtering, Plasma Etching, Plasma Enhanced CVD, Epitaxy, Electron Spectroscopies.	[9]
Plasma Science and Technology* Plasma Physics - Motion Of Individual Electrons and Ions In Electric And Magnetic Fields - Single, Collision Less, Particles In DC and AC Electric Fields, Particle Orbits In Magnetic Fields, Space Charge and Collective Effects, Debye Shielding, Plasma Oscillations and Plasma Freque,Ncy, Plasma Shielding And Plasma Sheaths, Response To DC, RF and Microwave Fields, Plasma Potential, Characteristic Electron and Ion Transit Times.	[9]
Advanced Plasma Reactor Technologies and Systems* Introduction to Plasma Reactors - Chamber Pump Systems, Load Locks, Mass Flow Control, Hazardous Gas Handling, Effluent Control, Pressure Gauges / Control (Piranhi, Thermocouple, Ionization, Baratron, Convectron) Wafer Chucks (Clamps/Electrostatic Chucks).	[9]
Advanced Rf and Microwave Plasma Interaction and Control* RF and Microwave Power Sources and Coupling - Power Sources, Matching Networks, Feedthroughs and Coupling RF Capacitively and Inductively Coupled Plasmas - Spatial Variations of Plasma Potential, Electric Field, Charge Density and Energy, Optical Emission, Sheaths at Powered, Grounded and Floating Surfaces, Parameters, Models, Matching Networks, Ion Bombardment - Energy / Time / Frequency/ Power Dependencies.	[9]
Thin-Film and Surface Processing Techniques* Common Analytical Methods For Surface and Thin Film, Processing Applications In Processes- Etching, Deposition, Sputtering, Ashing.	[9]
Total Hours:	**45**

Text Book(s):	
1.	V.V. Rao, T.B. Ghosh, K.L. Chopra,, “Vacuum Science and Technology”, Allied Publishers Ltd.,New Delhi.
2.	M. Sugawara, “Plasma Etching: Fundamentals and Applications: 7 (Series on Semiconductor Science and Technology)”- OUP Oxford.
Reference(s):	
1.	Dorothy M. Hoffman, Bawa Singh, John H. Thomas, “Handbook of Vacuum Science and Technology- III”, Academic Press.
2.	Karl Jousten, Wiley “Handbook of Vacuum Technology”
3.	Russ Morgan, Elsevier “Plasma Etching in Semiconductor Fabrication”
4.	J. A. Bittencourt “Fundamentals of Plasma Physics”, Springer India.
5.	Alexander Fridman, Lawrence Kennedy, “Plasma Physics and Engineering”, CRC Press

*SDG: 4 - Quality Education

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Fundamentals of Vacuum Technology**	
1.1	Introduction to Vacuum Technology	1
1.2	Gas Flow Calculations	1
1.3	Vacuum Pumps Technology- Diaphragm Pumps and Vacuum Blowers	1
1.4	Diffusion pumps, Cryogenic pumps	1
1.5	Pumps For Ultra-High Vacuum, Vacuum Measurements	1
1.6	Mass Analysis and Spectrometry, Mass Flow Control and Measurement	1
1.7	Vacuum Valves, Flanges and Components, Viewports	1
1.8	High-Vacuum-Based Processes: Sputtering, Plasma Etching	1
1.9	Plasma Enhanced CVD, Epitaxy, Electron Spectroscopies	1
2.0	**Plasma Science and Technology**	
2.1	Introduction to Plasma Physics	1
2.2	Particle Motion in Fields	1
2.3	Particle Orbits and Space Charge Effects	1
2.4	Debye Shielding and Plasma Oscillations	1
2.5	Plasma Sheaths and Shielding	1
2.6	Plasma in Different Fields	1
2.7	Plasma Potential and Transit Times	1
2.8	Collective Behaviour in Plasmas	1
2.9	Practical Applications of Plasma Physics	1
3.0	**Advanced Plasma Reactor Technologies and Systems**	
3.1	Introduction to Plasma Reactors	1
3.2	Load Locks and Mass Flow Control	1
3.3	Hazardous Gas Handling and Effluent Control	1
3.4	Pressure Gauges and Control	1
3.5	Wafer Chucks	1
3.6	Chamber Maintenance and Calibration	1
3.7	Advanced Pumping Techniques	1
3.8	System Diagnostics and Troubleshooting	1
3.9	Case Studies and Practical Examples	1
4.0	**Advanced RF and Microwave Plasma Interaction and Control**	
4.1	RF and Microwave Power Sources	1
4.2	Coupling Mechanisms	1
4.3	Capacitively and Inductively Coupled Plasmas	1
4.4	Spatial Variations in Plasma	1
4.5	Sheaths and Surface Interactions	1
4.6	Optical Emission and Diagnostics	1
4.7	Models and Parameters in Plasma	1
4.8	Ion Bombardment	1
4.9	Practical Control of Plasma Systems	1
5.0	**Thin-Film and Surface Processing Techniques**	
5.1	Common Analytical Methods for Surface and Thin Film processes	1
5.2	Etching Techniques	1
5.3	Deposition Techniques	1
5.4	Sputtering	1
5.5	Ashing and Cleaning Techniques	1
5.6	CVD and Epitaxy	1
5.7	Advanced Deposition Methods	1
5.8	Surface Characterization	1
5.9	Case Studies and Applications	1

Course Designer(s)

1. Saravanan S – saravanan.s@ksrct.ac.in

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60 EV E22	System Verilog	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the basic concept of system Verilog for verification
- to understand system Verilog basics and concepts
- to apply the concept of oops for verification
- to know the threads and inter - process communication and functional coverage
- to understand the purpose of hardware - software verification

Pre-requisites

- Verilog HDL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the concepts of verification methodologies	Understand
CO2	Summarize the concepts of data types and procedural statements	Understand
CO3	Illustrate the terminology and concept of OOPS for verification	Understand
CO4	Apply the concepts of inter-process communication between modules and functional coverage	Apply
CO5	Design a complete system model using system verilog	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	2	3	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	2	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	-	-	3	3	3	-	3	3	3	2
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	15
Understand	50	40	45
Apply	-	10	40
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E22 - System Verilog

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Verification Methodology Verification Guidelines - Verification Process - Verification Plan - Verification Methodology Manual-Test bench Functionality - Directed Testing - Methodology - Constrained Random Stimulus - Functional Coverage - Test bench Components - Layered Test bench.	[9]
System Verilog Data Types - Built in Data Types - Fixed Size Arrays - Dynamic Arrays – Queues - Creating New Types with Typedef - Creating User Defined Structures - Enumerated Types – Constants – Strings - Procedural Statements and Routines: Procedural Statements – Tasks – Functions - and Void Functions.	[9]
OOPS Creating New Objects - Object De allocation - Using Objects - Static Variables Vs. Global Variables - Class Routines - Defining Routines Outside of the Class - Scoping Rules - Using One Class Inside Another - Understanding Dynamic Objects - Copying Objects - Public Vs. Private - Straying Off Course - Building a Test bench – Inheritance – Polymorphism - Virtual Methods.	[9]
Threads and Inter-Process Communication and Functional Coverage Working with Threads - Inter Process Communication – Events – Semaphores – Mailboxes - Building a Testbench with Threads and IPC – Interface - Coverage Types - Functional Coverage Strategies - Simple Functional Coverage Example - Coverage Options - Parameterized Cover Groups - Analysing Coverage Data - Measuring Coverage Statistics.	[9]
Complete Design Model Using System Verilog- Case Study System Verilog ATM Example - Data Abstraction - Interface Encapsulation - Design Top Level Squat - Receivers and Transmitters - Test Bench for ATM*.	[9]
Total Hours:	**45**

Text Book(s):

1. Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, Springer 2008.
2. Janick Bergeron, “Writing Test benches: Functional Verification of HDL Models”, Kluwer Academic Publishers, Second Edition, 2003.

Reference(s):

1. Larry L. Peterson, Bruce S. Davie, “Computer Networks: A Systems Approach”, Morgan Kauffmann Publishers Inc., 2012.
2. Kurose James F and Keith W. Ross, “Computer Networking: A Top-Down Approach”, Pearson Education, 7th Edition, 2017.
3. Nataraj Venkataramanan, Ashwin Shriram,”Data Privacy: Principles and Practice”, CRC Press, 2016.
4. S. M. Ahsan Kazmi, Latif U. Khan, Choong Seon Hong, Nguyen H. Tran, “Network Slicing for 5G and Beyond Networks”, Springer International Publishing, 2020.

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Verification Methodology**	
1.1	Verification Guidelines	1
1.2	Verification Process, Verification Plan	1
1.3	Verification Methodology Manual	1
1.4	Test bench Functionality	1
1.5	Directed Testing	1
1.6	Methodology ,Constrained Random Stimulus	1
1.7	Functional Coverage	1
1.8	Test Bench Components	1
1.9	Layered Test Bench	1
2.0	**System Verilog**	
2.1	Data Types, Built in Data Types	1
2.2	Fixed Size Arrays, Dynamic Arrays	1
2.3	Queues	1
2.4	Creating New Types with Typedef	1
2.5	Creating User Defined Structures	1
2.6	Enumerated Types, Constants, Strings	1
2.7	Procedural Statements and Routines: Procedural Statements	1
2.8	Tasks and Functions, Void Functions	2
3.0	**OOPS**	
3.1	Creating New Objects	1
3.2	Object De allocation, Using Objects	1
3.3	Static Variables Vs. Global Variables	1
3.4	Class Routines, Defining Routines Outside of the Class	1
3.5	Scoping Rules, Using One Class Inside Another	1
3.6	Understanding Dynamic Objects, Copying Objects	1
3.7	Public Vs. Private, Straying Off Course	1
3.8	Building a Testbench, Inheritance	1
3.9	Polymorphism, Virtual Methods	1
4.0	**Threads And Inter-Process Communication And Functional Coverage**	
4.1	Working with Threads, Inter Process Communication	1
4.2	Events, Semaphores	1
4.3	Mailboxes	1
4.4	Building a Testbench with Threads and IPC	1
4.5	Interface, Coverage Types, Functional Coverage Strategies	1
4.6	Simple Functional Coverage Example	1
4.7	Coverage Options, Parameterized Cover Groups	1
4.8	Analysing Coverage Data	1
4.9	Measuring Coverage Statistics	1
5.0	**Complete Design Model Using System Verilog- Case Study**	
5.1	System Verilog ATM Example	2
5.2	Data Abstraction	1
5.3	Interface Encapsulation	1
5.4	Design Top Level Squat	1
5.5	Receivers and Transmitters	2
5.6	Test Bench for ATM	2

Course Designer(s)

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60 EV E23	Advanced Embedded Computing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To learn the embedded systems
- To study the embedded software development
- To learn the embedded system design with FPGA
- To discuss the internet of things and embedded systems
- To explore the embedded power management and advanced embedded computing

Pre-requisites

- Microprocessors and Microcontrollers

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the embedded systems	Understand
CO2	Analyse the embedded software development	Analyse
CO3	Examine the embedded system design with FPGA	Analyse
CO4	Interpret the internet of things and embedded systems	Understand
CO5	Analyse the embedded power management and advanced embedded computing	Analyse

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	-	2	2	2	-	-	-	2	3	3	3
CO2	3	3	3	-	-	2	2	2	-	-	-	2	3	3	3
CO3	3	3	3	-	-	2	2	2	-	-	-	2	3	3	3
CO4	3	3	3	-	-	2	2	2	-	-	-	2	3	3	3
CO5	3	3	3	-	-	2	2	2	-	-	-	2	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	20	20	30
Apply	-	-	-
Analyse	30	30	50
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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K.S.Rangasamy College of Technology – Autonomous R2022

B.E – Electronics Engineering (VLSI Design and Technology)

60 EV E23 - Advanced Embedded Computing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Embedded Systems *,**,*** Embedded Systems and Their Applications, Embedded System Design Constraints and Challenges, Review of Microcontrollers and Microprocessors, Real-Time Systems and Scheduling Algorithms, Features and Characteristics of RTOS, Task Scheduling, Synchronization, and Communication In RTOS	[9]
Embedded Software Development*,**,*** Software Development Tools and Environments for Embedded Systems, Embedded Software Architecture and Design Methodologies, Embedded Software Debugging and Testing Techniques, Interfacing Techniques For Embedded Systems, Serial Communication Protocols (UART, SPI, I2C), Parallel Interfaces (GPIO, DMA), Wireless Communication Standards (Bluetooth, Wi-Fi)	[9]
Embedded System Design with FPGA*,**,*** Field-Programmable Gate Arrays (FPGAs), FPGA Architecture and Programming Languages (Verilog, VHDL), Hardware - Software Co - Design Techniques, Embedded System Security Threats and Vulnerabilities, Security Measures In Embedded Systems (Encryption, Authentication), Secure Boot, Firmware Updates, and Secure Communication	[9]
Internet of Things (IoT) and Embedded Systems*,**,*** IoTConcepts and Architectures, Embedded Systems For IoT Applications (Sensor Nodes, Gateways), IoT Communication Protocols and Standards (MQTT, COAP), Signal Processing Algorithms For Embedded Systems, Digital Signal Processors (DSPs) and Their Applications, Real - Time Signal Processing Techniques	[9]
Embedded System Power Management*,**,*** Power Consumption Analysis In Embedded Systems, Low-Power Design Techniques (Power Gating, Voltage Scaling), Energy - Efficient Embedded System Architectures, Advanced Techniques: Edge Computing, Machine Learning on Embedded Devices and Neuromorphic Computing	[9]
Total Hours:	**45**

Text Book(s):

1.	Raj Kamal, "Embedded Systems: Architecture, Programming and Design", McGraw-Hill Education, 2017
2.	Jean J. Labrosse, "Real-Time Operating Systems Book 1: The Theory", Micrium Press, 2007

Reference(s):

1.	David E. Simon, "Embedded Software Primer", Addison-Wesley Professional, 2007
2.	Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-On Approach", VPT, 2014
3.	Steven W. Smith, "Digital Signal Processing: A Practical Guide for Engineers and Scientists", Newnes, 2002

*SDG 9 – Industry Innovation and Infrastructure
**SDG 3 – Good Health and Well Being
***SDG 11 – Sustainable Cities and Communities

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Embedded Systems**	
1.1	Embedded Systems and Their Applications	1
1.2	Embedded System Design Constraints and Challenges	1
1.3	Review of Microcontrollers and Microprocessors	2
1.4	Real-Time Systems and Scheduling Algorithms	2
1.5	Features And Characteristics of RTOS	1
1.6	Task Scheduling, Synchronization and Communication In RTOS	2
2.0	**Embedded Software Development**	
2.1	Software Development Tools and Environments for Embedded Systems	1
2.2	Embedded Software Architecture and Design Methodologies	1
2.3	Embedded Software Debugging and Testing Techniques	1
2.4	Interfacing Techniques for Embedded Systems	1
2.5	Serial Communication Protocols (UART, SPI, I2C)	2
2.6	Parallel Interfaces (GPIO, DMA)	2
2.7	Wireless Communication Standards (Bluetooth, Wi-Fi)	1
3.0	**Embedded System Design with FPGA**	
3.1	Field-Programmable Gate Arrays (Fpgas)	1
3.2	FPGA Architecture and Programming Languages (Verilog, VHDL)	1
3.3	Hardware-Software Co-Design Techniques	1
3.4	Embedded System Security Threats and Vulnerabilities,	2
3.5	Security Measures In Embedded Systems (Encryption, Authentication)	2
3.6	Secure Boot, Firmware Updates and Secure Communication	2
4.0	**Internet of Things (IoT) and Embedded Systems**	
4.1	IoT Concepts And Architectures	1
4.2	Embedded Systems for IoT Applications (Sensor Nodes, Gateways)	2
4.3	IoT Communication Protocols and Standards (MQTT, COAP)	2
4.4	Signal Processing Algorithms for Embedded Systems	1
4.5	Digital Signal Processors (DSPs) and Their Applications	1
4.6	Real-Time Signal Processing Techniques	2
5.0	**Embedded System Power Management**	
5.1	Power Consumption Analysis In Embedded Systems,	1
5.2	Low-Power Design Techniques (Power Gating, Voltage Scaling)	2
5.3	Energy-Efficient Embedded System Architectures	1
5.4	Edge Computing	1
5.5	Machine Learning on Embedded Devices	2
5.6	Neuromorphic Computing	2

Course Designer(s)

1. Dr.D. Mugilan - mugilan@ksrct.ac.in

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60 EV E24/60 EV L01	VLSI Technology	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To learn the VLSI design
- To study the CMOS technology
- To learn the physical design automation
- To discuss the advanced CMOS technologies
- To explore the analog and mixed signal VLSI design

Pre-requisites

- Digital Systems

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the VLSI design fabrication process	Understand
CO2	Discuss the CMOS technology	Understand
CO3	Analyse the physical design automation	Analyse
CO4	Explain the advanced CMOS technologies	Understand
CO5	Interpret the analog and mixed signal VLSI design	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	3	-	-	-	-	3	3	3	3
CO2	3	3	3	-	3	-	3	-	-	-	-	3	3	3	3
CO3	3	3	3	-	3	-	3	-	-	-	-	3	3	3	3
CO4	3	3	3	-	3	-	3	-	-	-	-	3	3	3	3
CO5	3	3	3	-	3	-	3	-	-	-	-	3	3	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	-	-
Understand	50	50	80
Apply	-	-	-
Analyse	-	10	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E – Electronics Engineering (VLSI Design and Technology)

60 EV E24/60 EV L01 – VLSI Technology

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

VLSI Design*,**,*** VLSI Technology and Its Applications - Historical Perspective and Evolution of VLSI Design - Semiconductor Materials and Properties - Crystal Structure and Doping, Carrier Concentration and Mobility.	[9]
CMOS Technology*,**,*** Complementary Metal-Oxide-Semiconductor (CMOS) Technology - Fabrication Process Steps (Oxidation, Lithography, Etching, Deposition) - CMOS Device Physics (MOSFET Operation: Threshold Voltage, Sub Threshold Conduction), Basic Building Blocks (Inverters, NAND/NOR Gates, Transmission Gates) - Static and Dynamic Logic Families- Combinational and Sequential Circuit Design.	[9]
Physical Design Automation*,**,*** Physical Design Automation (Pda) Tools And Methodologies: Floor Planning, Placement, And Routing Techniques, Timing Analysis and Optimization - VLSI Testing Techniques (Scan Chains, Built-In Self-Test) - Design For Testability (DFT) Principles - Functional Verification Techniques.	[9]
Advanced CMOS Technologies*,**,*** Deep Submicron CMOS Technology - FinFET And Multi-Gate Transistor Technology - Emerging Technologies (Nanotechnology, Quantum Computing) - Power Consumption Sources In CMOS Circuits - Power Optimization Techniques (Clock Gating, Voltage Scaling, Power Gating) - Low Power Design Methodologies.	[9]
Analog and Mixed-Signal VLSI Design*,**,*** Analog and Mixed-Signal VLSI Design, Basic Analog Building Blocks (Amplifiers, Oscillators, Filters), Analog-To-Digital And Digital-To-Analog Converters (Adcs/Dacs), Hands-On Experience With VLSI Design Tools .	[9]
Total Hours:	**45**

Text Book(s):	
1.	Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson, 2002
2.	Tony Chan Carusone, David A. Johns, and Kenneth W. Martin, "Analog Integrated Circuit Design", Wiley, 2011
Reference(s):	
1.	Alan Hastings and Roy Alan Hastings, "The Art of Analog Layout", Prentice Hall, 2000
2.	Author: Neil H. E. Weste and David Money Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison-Wesley, 2010
3.	Thomas D. Caronna, "VLSI Design Methodology Development", CRC press, 2018
4.	Sadiq M. Sait and Habib Youssef, "Physical Design Automation of VLSI Systems" , CRC Peess, 1999

*SDG 9 – Industry Innovation and Infrastructure
**SDG 3 – Good Health and Well Being
***SDG 11 – Sustainable Cities and Communities

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**VLSI Design**	
1.1	VLSI Technology and Its Applications,	2
1.2	Historical Perspective and Evolution Of VLSI Design	1
1.3	Semiconductor Materials and Properties	2
1.4	Crystal Structure and Doping	2
1.5	Carrier Concentration and Mobility	2
2.0	**CMOS Technology**	
2.1	Complementary Metal-Oxide-Semiconductor (CMOS) Technology	1
2.2	Fabrication Process Steps (Oxidation, Lithography, Etching, Deposition)	2
2.3	CMOS Device Physics (MOSFET Operation, Threshold Voltage	1
2.4	Sub Threshold Conduction)	1
2.5	Building Blocks (Inverters, NAND/NOR Gates, Transmission Gates)	1
2.6	Static and Dynamic Logic Families	1
2.7	Combinational and Sequential Circuit Design	2
3.0	**Physical Design Automation**	
3.1	Physical Design Automation (PDA) Tools and Methodologies	1
3.2	Floor Planning, Placement and Routing Techniques	2
3.3	Timing Analysis and Optimization	2
3.4	VLSI Testing Techniques (Scan Chains, Built-In Self-Test)	2
3.5	Design for Testability (DFT) Principles	1
3.6	Functional Verification Techniques	1
4.0	**Advanced CMOS Technologies**	
4.1	Deep Submicron CMOS Technology	1
4.2	Finfet and Multi-Gate Transistor Technology	2
4.3	Emerging Technologies (Nanotechnology, Quantum Computing)	2
4.4	Power Consumption Sources In CMOS Circuits	1
4.5	Power Optimization Techniques (Clock Gating, Voltage Scaling, Power Gating)	2
4.6	Low Power Design Methodologies	1
5.0	**Analog and Mixed-Signal VLSI Design**	
5.1	Analog and Mixed-Signal VLSI Design	1
5.2	Analog Building Blocks (Amplifiers, Oscillators, Filters)	2
5.3	Analog-To-Digital And Digital-To-Analog Converters (Adcs/Dacs)	2
5.4	Hands-On Experience With VLSI Design Tools	4

Course Designer(s)

1. Dr.D. Mugilan - mugilan@ksrct.ac.in

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60 EV E26	Digital Image Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the concept of digital image fundamentals
- To learn about simple image enhancement techniques in Spatial and Frequency domain
- To explain the concepts of degradation function and restoration techniques
- To study the image segmentation and representation techniques
- To learn the concept of image compression and recognition methods

Pre-requisites

- Basic knowledge of Electrical and Electronics Engineering

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the fundamentals of image.	Remember
CO2	Discuss image enhancement techniques in spatial domain.	Understand
CO3	Analyse image restoration through various filters	Apply
CO4	Apply the concepts of segmentation.	Apply
CO5	Discuss the algorithms for lossy and lossless compression.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO2	3	3	3	-	3	-	-	-	3	3		3	3	2	3
CO3	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO4	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO5	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	34
Understand	40	20	51
Apply	-	20	15
Analyse	-	-	-
Evaluate	-	-	-
Create	10	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E26 - Digital Image Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Digital Image Fundamentals and Transforms* Elements of Visual Perception – Image Sampling and Quantization Basic Relationship Between Pixels – Basic Geometric Transformations - Fourier Transform and DFT – Properties of 2D Fourier Transform – Discrete Cosine Transform, Haar, Color Image Fundamentals - RGB, HSI Models.	[9]
Image Enhancement* Basic Gray Level Transformations – Histogram Equalization – Histogram Matching –Spatial Filtering – Smoothing Spatial Filters – Sharpening Spatial Filters- Ideal, Butterworth And Gaussian Filters, Homomorphic Filtering, Color Image Enhancement. **Hands on:** Simulation of Image Enhancement	[9]
Restoration* Model Of The Image Degradation / Restoration Process- Mean Filters – Order – Statistics Filters- Adaptive Filters – Inverse Filtering – Minimum Mean Square Error Filtering – Constrained Least Squares Filtering – Geometric Mean Filter – Geometric Transformations.	[9]
Image Segmentation and Representation* Edge Detection – Thresholding – Region Based Segmentation – Boundary Representation: Chair Codes- Polygonal Approximation – Boundary Segments – Boundary Descriptors: Simple Descriptors - Fourier Descriptors – Regional Descriptors –Simple Descriptors- Texture Image Segmentation Based on Color. **Hands on:** Simulation of Image Segmentation	[9]
Image Compression* Lossless Compression: Variable Length Coding – LZW Coding – Bit Plane Coding- Predictive Coding - DPCM. Lossy Compression: Transform Coding – Wavelet Coding – Basics of Image Compression Standards: JPEG, MPEG, Basics of Vector Quantization. **Hands on:** Simulation of Image Compression	[9]
Total Hours:	**45**

Text Book(s):

1.	Rafael C Gonzalez, Richard E. Woods, “Digital Image Processing”, 4th Edition, Pearson Education, 2018.
2.	A.K. Jain, “Fundamentals of Digital Image Processing”, New Edition, Prentice Hall of India, 2016.

Reference(s):

1.	Rafael C Gonzalez, Richard E. Woods, “Digital Image Processing”, Prentice Hall, 3rd Edition, 2016.
2.	William K. Pratt, “Digital Image Processing”, John Wiley, New York, 2016.
3.	D.E. Dudgeon and RM. Mersereau, “Multidimensional Digital Signal Processing”, Prentice Hall Professional Technical Reference, 2016.
4.	Yao Wang, JoernOstermann, and Ya-Qin Zhang, “Video Processing and Communications”, Prentice Hall, 2016.

*SDG: 4- Quality Education

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Course Contents and Lecture Schedule

S.No.	Topic	No. of Hours
1.0	**Digital Image Fundamentals and Transforms**	
1.1	Steps In Digital Image Processing	1
1.2	Elements of Visual Perception	1
1.3	Image Sensing And Acquisition	1
1.4	Image Sampling And Quantization	1
1.5	Relationships Between Pixels	1
1.6	Color Image Fundamentals	1
1.7	RGB, HSI Models,	1
1.8	Two-Dimensional Mathematical Preliminaries	1
1.9	2D Transforms - DFT, DCT	1
2.0	**Image Enhancement**	
2.1	Basic Gray Level Transformations	2
2.2	Histogram Processing	1
2.3	Histogram Matching	1
2.4	Spatial Filtering	1
2.5	Smoothing Spatial Filters	1
2.6	Sharpening Spatial Filters	1
2.7	Homomorphic Filtering	1
2.8	Color Image Enhancement	1
3.0	**Restoration**	
3.1	Model of The Image Degradation / Restoration Process	1
3.2	Mean Filters	1
3.3	Order Statistics Filters	2
3.4	Adaptive Filters	1
3.5	Inverse Filtering	1
3.6	Minimum Mean Square Error Filtering	1
3.7	Constrained Least Squares Filtering	1
3.8	Geometric Mean Filter	1
4.0	**Image Segmentation**	
4.1	Edge Detection	1
4.2	Thresholding	1
4.3	Region Based Segmentation Region Based Segmentation	1
4.4	Region Growing	1
4.5	Region Splitting And Merging	1
4.6	Morphological Processing	1
4.7	Erosion and Dilation	1
4.8	Segmentation By Morphological Watersheds	2
5.0	**Image Compression and Recognition**	
5.1	Need For Data Compression,	1
5.2	Huffman, Run Length Encoding Codes	1
5.3	Arithmetic Coding	1
5.4	JPEG Standard, Boundary Representation	1
5.5	Boundary Description,	1
5.6	Fourier Descriptor, Regional Descriptors	1
5.7	Topological Feature, Texture	1
5.8	Patterns and Pattern Classes	1
5.9	Recognition Based on Matching	1
	Total	**45**

Course Designer(s)

1. Dr.S.Malarkhodi – Malarkhodi@ksrct.ac.in

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60 EV E26	Digital Image Processing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the concept of digital image fundamentals
- To learn about simple image enhancement techniques in Spatial and Frequency domain
- To explain the concepts of degradation function and restoration techniques
- To study the image segmentation and representation techniques
- To learn the concept of image compression and recognition methods

Pre-requisites

- Basic knowledge of Electrical and Electronics Engineering

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the fundamentals of image.	Remember
CO2	Discuss image enhancement techniques in spatial domain.	Understand
CO3	Analyse image restoration through various filters	Apply
CO4	Apply the concepts of segmentation.	Apply
CO5	Discuss the algorithms for lossy and lossless compression.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO2	3	3	3	-	3	-	-	-	3	3		3	3	2	3
CO3	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO4	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
CO5	3	3	3	-	3	-	-	-	3	3	-	3	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	20	20	34
Understand	40	20	51
Apply	-	20	15
Analyse	-	-	-
Evaluate	-	-	-
Create	10	-	-
Total	60	60	100

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B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E26 - Digital Image Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VI	3	0	0	45	3	40	60	100

Digital Image Fundamentals and Transforms* Elements of Visual Perception – Image Sampling and Quantization Basic Relationship Between Pixels – Basic Geometric Transformations - Fourier Transform and DFT – Properties of 2D Fourier Transform – Discrete Cosine Transform, Haar, Color Image Fundamentals - RGB, HSI Models.	[9]
Image Enhancement* Basic Gray Level Transformations – Histogram Equalization – Histogram Matching –Spatial Filtering – Smoothing Spatial Filters – Sharpening Spatial Filters- Ideal, Butterworth And Gaussian Filters, Homomorphic Filtering, Color Image Enhancement. **Hands on:** Simulation of Image Enhancement	[9]
Restoration* Model Of The Image Degradation / Restoration Process- Mean Filters – Order – Statistics Filters- Adaptive Filters – Inverse Filtering – Minimum Mean Square Error Filtering – Constrained Least Squares Filtering – Geometric Mean Filter – Geometric Transformations.	[9]
Image Segmentation and Representation* Edge Detection – Thresholding – Region Based Segmentation – Boundary Representation: Chair Codes- Polygonal Approximation – Boundary Segments – Boundary Descriptors: Simple Descriptors - Fourier Descriptors – Regional Descriptors –Simple Descriptors- Texture Image Segmentation Based on Color. **Hands on:** Simulation of Image Segmentation	[9]
Image Compression* Lossless Compression: Variable Length Coding – LZW Coding – Bit Plane Coding- Predictive Coding - DPCM. Lossy Compression: Transform Coding – Wavelet Coding – Basics of Image Compression Standards: JPEG, MPEG, Basics of Vector Quantization. **Hands on:** Simulation of Image Compression	[9]
Total Hours:	**45**

Text Book(s):	
1.	Rafael C Gonzalez, Richard E. Woods, “Digital Image Processing”, 4th Edition, Pearson Education, 2018.
2.	A.K. Jain, “Fundamentals of Digital Image Processing”, New Edition, Prentice Hall of India, 2016.
Reference(s):	
1.	Rafael C Gonzalez, Richard E. Woods, “Digital Image Processing”, Prentice Hall, 3rd Edition, 2016.
2.	William K. Pratt, “Digital Image Processing”, John Wiley, New York, 2016.
3.	D.E. Dudgeon and RM. Mersereau, “Multidimensional Digital Signal Processing”, Prentice Hall Professional Technical Reference, 2016.
4.	Yao Wang, JoernOstermann, and Ya-Qin Zhang, “Video Processing and Communications”, Prentice Hall, 2016.

*SDG: 4- Quality Education

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Course Contents and Lecture Schedule

S.No.	Topic	No. of Hours
1.0	**Digital Image Fundamentals and Transforms**	
1.1	Steps In Digital Image Processing	1
1.2	Elements of Visual Perception	1
1.3	Image Sensing And Acquisition	1
1.4	Image Sampling And Quantization	1
1.5	Relationships Between Pixels	1
1.6	Color Image Fundamentals	1
1.7	RGB, HSI Models,	1
1.8	Two-Dimensional Mathematical Preliminaries	1
1.9	2D Transforms - DFT, DCT	1
2.0	**Image Enhancement**	
2.1	Basic Gray Level Transformations	2
2.2	Histogram Processing	1
2.3	Histogram Matching	1
2.4	Spatial Filtering	1
2.5	Smoothing Spatial Filters	1
2.6	Sharpening Spatial Filters	1
2.7	Homomorphic Filtering	1
2.8	Color Image Enhancement	1
3.0	**Restoration**	
3.1	Model of The Image Degradation / Restoration Process	1
3.2	Mean Filters	1
3.3	Order Statistics Filters	2
3.4	Adaptive Filters	1
3.5	Inverse Filtering	1
3.6	Minimum Mean Square Error Filtering	1
3.7	Constrained Least Squares Filtering	1
3.8	Geometric Mean Filter	1
4.0	**Image Segmentation**	
4.1	Edge Detection	1
4.2	Thresholding	1
4.3	Region Based Segmentation Region Based Segmentation	1
4.4	Region Growing	1
4.5	Region Splitting And Merging	1
4.6	Morphological Processing	1
4.7	Erosion and Dilation	1
4.8	Segmentation By Morphological Watersheds	2
5.0	**Image Compression and Recognition**	
5.1	Need For Data Compression,	1
5.2	Huffman, Run Length Encoding Codes	1
5.3	Arithmetic Coding	1
5.4	JPEG Standard, Boundary Representation	1
5.5	Boundary Description,	1
5.6	Fourier Descriptor, Regional Descriptors	1
5.7	Topological Feature, Texture	1
5.8	Patterns and Pattern Classes	1
5.9	Recognition Based on Matching	1
	Total	**45**

Course Designer(s)

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60 EV E31	Low Power VLSI Design	Category	L	T	P	C
		PE	2	0	2	3

Objectives

- Understand the fundamental principles of low-power design for digital circuits, focusing on CMOS technology.
- Equips with techniques to minimize power consumption from fundamental building blocks to complex systems.
- Identify suitable techniques to arrange the physical layout of the circuit for better power efficiency.
- Familiarize power estimation techniques for digital circuits across various abstraction levels.
- Acquire knowledge on algorithms for power-efficient design techniques.

Pre-requisites

- Electronic Circuit, VLSI Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Analyze power consumption in digital circuits and apply techniques to minimize it.	Analyze
CO2	Apply the power minimization in design of low power VLSI subsystem on CMOS.	Apply
CO3	Design low-power arithmetic circuits by optimizing logic, memory, clocks, and physical layout.	Apply
CO4	Predict and analyze power consumption in digital designs using circuit, gate, architecture, and behavioural methods.	Apply
CO5	Apply power-aware transformations and software design techniques.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	3	1	-	-	-	-	-	-	-	-	3	-	-
CO3	3	3	3	2	-	-	-	-	-	-	-	-	3	-	-
CO4	-	3	3	-	-	-	-	-	-	-	-	-	3	-	-
CO5	-	3	3	-	3	-	-	-	-	-	-	-	3	-	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Exam (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	10	-	10	-	20	-	20
Understand	30	-	30	-	50	-	50
Apply	20	50	20	50	30	50	30
Analyse	-	50	-	50	-	50	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S. Rangasamy College of Technology - Autonomous R2022

B.E - Electronics Engineering (VLSI Design & Technology)

60 EV E31 - Low Power VLSI Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

Power Dissipation In CMOS* Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.	[6]
Power Optimization* Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design.	[6]
Design of Low Power CMOS Circuits* Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – – Physical Design, Floor Planning, Placement and Routing.	[6]
Power Estimation* Power Estimation Techniques, Circuit Level, Gate Level, Behavioural Level, – Logic Power Estimation – Simulation Power Analysis	[6]
Synthesis and Software Design for Low Power CMOS Circuits* Synthesis for Low Power – Behavioural Level Transform – Algorithms for Low Power – Software Design for Low Power.	[6]
Practical: 1. Design a simple inverter circuit with different load capacitances and observe the change in dynamic power consumption with varying CL. 2. Simulate the simple logic circuits and analyse the trade-off between dynamic power reduction and circuit speed with varying Vdd. 3. Analyze power reduction through logic minimization techniques (e.g., Karnaugh Map simplification) using a Hardware Description Language (HDL) simulator. 4. Investigate the trade-off between dynamic power and delay by simulating inverters with different transistor sizes in a SPICE simulator. 5. Implement and compare the power consumption of non-pipelined and pipelined multipliers in an HDL simulator. 6. Design and compare the power consumption of ripple carry adders and CSAs using an HDL simulator. Analyze the impact of operand bit width on power efficiency. 7. Design an FSM with different state encoding schemes (e.g., one-hot vs. binary) and compare their power consumption using a synthesis tool. 8. Implement a multiplier in an HDL and explore power reduction through logic minimization techniques (e.g., using a compressor tree) while maintaining accuracy. 9. Design a circuit with clock gating and analyse its impact on dynamic power consumption using a power analysis tool. Explore the trade-off with performance by varying the clock frequency. 10. Design a combinational circuit in an HDL and simulate it with different input vectors using a logic simulator. Analyze the switching activity of internal nodes and explore its correlation with power consumption.	[30]
Total Hours: (Lecture - 30; Practical - 30)	**60**

Text Book(s):

1.	Roy, Kaushik, and Sharat C. Prasad, “Low-power CMOS VLSI circuit design”. John Wiley & Sons, 2009.
2.	Piguet, Christian. “Low-power CMOS circuits: technology, logic design and CAD tools”, CRC press, 2018.

Reference(s):

1.	James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001
2.	J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 1999.
3.	Yeap, Gary K. “Practical low power digital VLSI design”, Springer Science & Business Media, 2012.
4.	Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic,” Digital Integrated Circuits: A Design Perspective”, 2nd edition, Pearson Publications, 2003.

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Power Dissipation In CMOS**	
1.1	Hierarchy of limits of power: System Level, Architectural Level, Circuit Level	1
1.2	Hierarchy of limits of power: Logic Level, Gate Level, Device Level	1
1.3	Sources of Power Consumption: Static and Dynamic power consumption, concepts and derivation	1
1.4	Sources of Power Consumption: short circuit and leakage power consumption, concepts and derivation	1
1.5	Physics of Power Dissipation in CMOS FET Devices: CMOS technology overview, sources of power dissipation	1
1.6	Basic Principle of Low Power Design: Low power Design, Power analysis and modelling, static and dynamic power reduction	1
2	**Power Optimization**	
2.1	Logic Level Power Optimization & Circuit Level Low Power Design	2
2.2	Gate Level Low Power Design: Power, Domain, resource sharing, power management	1
2.3	Architecture Level Low Power Design: Concept and optimization techniques	1
2.4	VLSI Subsystem Design of Adders, Multipliers: Concept, methodology and power optimization	1
2.5	PLL, Low Power Design: PLL working, design methodology, low power design	1
3	**Design of Low Power CMOS Circuits**	
3.1	Computer Arithmetic Techniques for Low Power System- Concept, Methods and Types	1
3.2	Reducing Power Consumption in Combinational Logic- Design Methodology and Analysis	1
3.3	Reducing Power Consumption in Sequential Logic and Memories – Design methodology and analysis	1
3.4	Low Power Clock & Advanced Techniques – Techniques for low power design	1
3.5	Physical Design, Floor Planning	1
3.6	Placement and Routing: Concept and necessity in low power design	1
4	**Power Estimation**	
4.1	Circuit and Gate Level power estimation techniques	1
4.2	Architectural Level power estimation techniques	1
4.3	Behavioral Level power estimation techniques	1
4.4	Logic Power Estimation and its methodology	1
4.5	Simulation Power Analysis – Concept and Methodology	2
5	**Synthesis and Software Design for Low Power CMOS Circuits**	
5.1	Synthesis for Low Power – Overview, Optimization and Synthesis	1
5.2	Behavioral Level Transform- functionality in terms of operations, interaction and optimization	1
5.3	Algorithms for Low Power -DVFS, Task Scheduling and Allocation	1
5.4	Algorithms for Low Power- AVS, Power Routing and signal processing	1
5.5	Software Design for Low Power -Techniques for low power computing at software level	1
5.6	Software Design for Low Power – Analysis of various low power computing techniques	1
	Practical:	
1.	Design a simple inverter circuit with different load capacitances and observe the change in dynamic power consumption with varying CL.	3
2.	Simulate the simple logic circuits and analyse the trade-off between dynamic power reduction and circuit speed with varying Vdd.	3
3.	Analyze power reduction through logic minimization techniques (e.g., Karnaugh Map simplification) using a Hardware Description Language (HDL) simulator.	3
4.	Investigate the trade-off between dynamic power and delay by simulating inverters with different transistor sizes in a SPICE simulator.	3
5.	Implement and compare the power consumption of non-pipelined and pipelined multipliers in an HDL simulator.	3
6.	Design and compare the power consumption of ripple carry adders and CSAs using an HDL simulator. Analyze the impact of operand bit width on power efficiency.	3
7.	Design an FSM with different state encoding schemes (e.g., one-hot vs. binary) and compare their power consumption using a synthesis tool.	3
8.	Implement a multiplier in an HDL and explore power reduction through logic minimization techniques (e.g., using a compressor tree) while maintaining accuracy.	3
9.	Design a circuit with clock gating and analyse its impact on dynamic power consumption using a power analysis tool. Explore the trade-off with performance by varying the clock frequency.	3
10.	Design a combinational circuit in an HDL and simulate it with different input vectors using a logic simulator.	3

Course Designer(s)

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60 EV E32	VLSI Signal Processing	Category	L	T	P	C
		PE	2	0	2	3

Objectives

- To build low-power digital filters using techniques like pipelining, parallelization, and retiming.
- To analyze retiming and unfolding techniques to increase the throughput of the circuit.
- To explore resource usage with folding transformations, while minimizing register needs in those designs.
- To equip to design High-speed processors for signal processing
- To emphasis on architecture design based on design methodologies for mapping algorithms to arithmetic architectures at bit-level

Pre-requisites

- Signals and Systems, Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explore techniques for designing low-power digital filters, focusing on pipelining, parallel processing, and retiming of FIR filters.	Analyze
CO2	Optimizing digital filter designs, including unfolding algorithms, critical path analysis, and retiming for low-power and potentially reduced algorithmic complexity.	Analyze
CO3	Applying folding transformations to reduce resource usage while exploring methods to minimize register requirements in folded architectures, including multirate systems.	Apply
CO4	Design efficient hardware architectures like systolic arrays for FIR filters, matrix multiplication, and more, leveraging spatial representations with delays.	Apply
CO5	Design and implement bit-level arithmetic architectures and bit-parallel multipliers.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	-	-	3
CO2	2	2	-	-	-	-	-	-	-	-	-	-	-	-	3
CO3	3	-	-	2	-	-	-	-	-	-	-	-	-	-	3
CO4	3	2	-	-	-	-	-	-	-	-	-	-	-	-	3
CO5	3	-	-	2	-	-	-	-	-	-	-	-	-	-	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Exam (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	10	-	10	-	20	-	20
Understand	25	-	25	-	40	-	40
Apply	15	50	15	50	25	50	25
Analyse	10	50	10	50	15	50	15
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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B.E - Electronics Engineering (VLSI Design & Technology)

60 EV E32 - VLSI Signal Processing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

Pipelining and Parallel Processing* Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Retiming Techniques.	[6]
Unfolding* Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding Algorithmic Strength Reduction in Filters and Transforms.	[6]
Folding* Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	[6]
Systolic Architecture Design* Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication, Systolic Design for Space Representations Containing Delays.	[6]
Bit-Level Arithmetic Architecture* Bit-level architecture – Introduction, Parallel Multipliers, Parallel Multiplication with sign extension, Parallel Carry-ripple Array Multipliers, Baugh-Wooley Multipliers, Parallel Multipliers with Modified Booth Recoding.	[6]
Practical: 1. Design and implement an FIR filter on a hardware platform (e.g., FPGA, DSP board). 2. Modify the filter architecture by inserting pipeline stages and analyse the impact on performance. 3. Experiment with retiming the filter to improve performance or reduce register count. 4. Investigate how retiming can be used in conjunction with unfolding to further optimize the critical path of filter design. 5. Apply different unfolding technique (loop unrolling, GU) algorithm for filter design and analyse the impact on performance. 6. Performance Enhancement through Folding Transformation in DSP Systems. 7. Design and implementation of Systolic Array Design for FIR Filters and Matrix Multiplication. 8. Design and implementation of fast convolution for DSP System using Cook-Toom Algorithms. 9. Design and Implementation of Baugh-Wooley Multipliers for Signed Binary Multiplication. 10. Design and Simulation of Parallel Multipliers with Sign Extension.	[30]
Total Hours: (Lecture - 30; Practical - 30)	**60**

Text Book(s):

1.	Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2.	K.K. Parhi and T. Nishitani, "Digital Signal Processing for Multimedia Systems", CRC Press,1999.

Reference(s):

1.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
2.	S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
3.	Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
4.	John L. Hennessy, David A. Patterson," Computer Architecture: A Quantitative Approach", 6th Edition, Elsevier, 2017.

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of Hours**
1	**Pipelining and Parallel Processing**	
1.1	Pipelining of FIR Digital Filters and parallel processing – Concept and Design	1
1.2	Pipelining of FIR Digital Filters and parallel processing - Concept and Design	1
1.3	Pipelining and Parallel Processing for Low Power – Design and Methodologies	1
1.4	Pipelining and Parallel Processing for Low Power – Design and Methodologies	1
1.5	Retiming: Introduction, Definition and Properties	1
1.6	Retiming Techniques – Methodologies and implementation	1
2	**Unfolding**	
2.1	Introduction an Algorithms for Unfolding	1
2.2	Properties of Unfolding and Critical Path	1
2.3	Unfolding and Retiming	1
2.4	Application of Unfolding Algorithmic Strength Reduction in Filters	1
2.5	Application of Unfolding Algorithmic Strength Reduction in Filters	1
2.6	Application of Unfolding Algorithmic Strength Reduction in Transforms.	1
3	**Folding**	
3.1	Introduction to Folding Transformation	1
3.2	Register Minimization Techniques	1
3.3	Register Minimization in Folded Architectures	1
3.4	Register Minimization in Folded Architectures	1
3.5	Folding in Multirate Systems	1
3.6	Folding in Multirate System.	1
4	**Systolic Architecture Design**	
4.1	Introduction, Systolic Array Design Methodology	1
4.2	FIR Systolic Arrays	1
4.3	Selection of Scheduling Vector	1
4.4	Matrix Multiplication	1
4.5	Systolic Design for Space Representations	1
4.6	Systolic Design for Space Representations Containing Delays	1
5	**Bit Level Arithmetic Architectures**	
5.1	Bit-level architecture	1
5.2	Introduction and Parallel Multipliers	1
5.3	Parallel Multiplication with sign extension	1
5.4	Parallel Carry-ripple Array Multipliers	1
5.5	Baugh-Wooley Multipliers,	1
5.6	Parallel Multipliers with Modified Booth Recoding	1
Practical:		
1.	Design and implement an FIR filter on a hardware platform (e.g., FPGA, DSP board).	3
2.	Modify the filter architecture by inserting pipeline stages and analyse the impact on performance.	3
3.	Experiment with retiming the filter to improve performance or reduce register count.	3
4.	Investigate how retiming can be used in conjunction with unfolding to further optimize the critical path of filter design.	3
5.	Apply different unfolding technique (loop unrolling, GU) algorithm for filter design and analyse the impact on performance.	3
6.	Performance Enhancement through Folding Transformation in DSP Systems.	3
7.	Design and implementation of Systolic Array Design for FIR Filters and Matrix Multiplication.	3
8.	Design and implementation of fast convolution for DSP System using Cook-Toom Algorithms.	3
9.	Design and Implementation of Baugh-Wooley Multipliers for Signed Binary Multiplication.	3
10.	Design and Simulation of Parallel Multipliers with Sign Extension.	3

Course Designer(s)

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60 EV E33	Scripting Languages for VLSI Design Automation	Category	L	T	P	Credit
		PE	2	0	2	3

Objectives

- To Understand the basic features of TCL
- To Construct TCL scripts for EDA
- To Identify the basic constructs in Tk
- To Explain the basic concepts of Python
- To Summarize the advanced features of Python

Pre-requisites

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the basic features of TCL	Understand
CO2	Illustrate the advanced features of TCL scripting language	Understand
CO3	Demonstrate the concepts of TK	Apply
CO4	Explain the basics of Python	Understand
CO5	Describe the advanced concepts of Python to write the script for automation	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Exam (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	15	-	-	30	-
Understand	40	20	30	10	10	50	10
Apply	-	80	15	90	90	20	90
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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B.E - Electronics Engineering (VLSI Design & Technology)

60 EV E33 – Scripting Languages for VLSI Design Automation

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

TCL* Tool Command Language (TCL), Language Syntax, Variables, Expressions-String Processing –TCL Lists-Control Structure Command-Procedure and Scope-TCL Arrays.	[6]
Advanced TCL* Quoting Issues and Regular Expressions-Script Libraries and Packages - Reflection and Debugging - Namespaces-Internationalization - Event Driven Programming - Socket Programming.	[6]
Tool Kit* TK(Tool Kit) - The Pack Geometry Manager, The Grid Geometry Manager, The Place Geometry Manager, Binding Commands To Events - TK Widgets.	[6]
Python* Python Interpreter and Interactive Mode, Debugging; Values and Types: Int, Float, Boolean, String, and List; Variables, Expressions, Statements, Tuple Assignment, Precedence of Operators, Comments; Illustrative Programs: Exchange the Values of Two Variables, Circulate the Values of N Variables, Distance Between Two Points.	[6]
Lists, Tuples, Dictionaries* Lists: List Operations, List Slices, List Methods, List Loop, Mutability, Aliasing, Cloning Lists, List Parameters; Tuples: Tuple Assignment, Tuple as Return Value; Dictionaries: Operations and Methods; Advanced List Processing - List Comprehension; Illustrative Programs: Simple Sorting, Histogram, Students Marks Statement, Retail Bill Preparation.	[6]
Practical: 1. Write a TCL script to find the factorial of a number 2. Write a TCL script that multiplies the numbers from 1 to 10 3. Write a TCL script for Sorting a list using a comparison function 4. Write a TCL script to comparing the file modified times. 5. Write a TCL script to Copy a file and translate to native format 6. Python programming using simple statements and expressions (exchange the values of two variables, circulate the values of n variables, distance between two points). 7. Scientific problems using Conditionals and Iterative loops. (Number series, Number Patterns, pyramid pattern) 8. Implementing real-time/technical applications using Lists, Tuples. (Items present in a library/Components of a car/ Materials required for construction of a building –operations of list & tuples) **Tools used: VLSI EDA Tool**	[30]
Total Hours: (Lecture - 30; Practical - 30)	**60**
Text Book(s):	

1.	John K. Ousterhout, Ken Jones, “Tcl and the Tk Toolkit”, Pearson Education, Second Edition, 2010.
2.	Chromatic “Modern Perl “Fourth Edition, 2015
Reference(s):	
1.	LarryWall, Tom Christiansen, John want, “Programming PERL”, Oreilly publications, 4th ed 2012
2.	Naveed Sherwani, Algorithms for VLSI physical design Automation, Kluwer Academic Publishers,2013.
3.	Brent Welch,"Practical Programming in Tcl and Tk",Fourth Edition, 2003.
4.	David Barron, "The World of Scripting Languages", Wiley Publications, 2000.

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Course Contents and Lecture Schedule		
S. No.	**Topics**	**No. of hours**
1.0	**TCL**	
1.1	Tool Command Language (TCL)	1
1.2	Language syntax, variables, expressions	1
1.3	String processing	1
1.4	TCL Lists-control structure command	1
1.5	Procedure and scope	1
1.6	TCL arrays	1
2.0	**Advanced TCL**	
2.1	Quoting issues and Regular expressions	1
2.2	Script libraries and Packages	1
2.3	Reflection and debugging	1
2.4	Namespaces-Internationalization	1
2.5	Event driven programming	1
2.6	Socket programming	1
3.0	**Tool Kit**	
3.1	TK(Tool Kit)	1
3.2	The pack geometry manager	1
3.3	The grid geometry manager	1
3.4	The place geometry manager	1
3.5	Binding commands to events	1
3.6	TK widgets	1
4.0	**Python**	
4.1	Python interpreter and interactive mode, debugging; values and types	1
4.2	Int, float, boolean, string, and list; variables	1
4.3	Expressions, statements, tuple assignment, precedence of operators, comments;	1
4.4	Illustrative programs: exchange the values of two variables	1
4.5	circulate the values of n variables	1
4.6	distance between two points	1
5.0	**Lists, Tuples, Dictionaries**	
5.1	Lists	2
5.2	Tuples	2
5.3	advanced list processing	1
5.4	Illustrative programs	1

Course Designer(s)

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Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV E34	System on Chip	Category	L	T	P	Credit
		PE	2	0	2	3

Objectives

- To introduce architecture and design concepts underlying system on chips.
- To explain the knowledge of designing SoCs.
- To learn impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications.
- To learn the modelling, synthesis, and physical design.
- To learn the various FPGA base Embedded Processor

Pre-requisites

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Illustrate all important components of a System-on-Chip and an embedded system	Understand
CO2	Learn the digital hardware and Embedded software	Understand
CO3	Examine the major design flows for digital hardware and embedded software	Apply
CO4	Describe the major architectures and trade-offs concerning performance, cost and power	Understand
CO5	Outline the Consumption of single chip and embedded systems	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	2	3	-	-	-	-	-	-	3	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	3	3	3	-
CO3	3	3	3	2	2	-	-	-	-	-	-	3	3	3	-
CO4	3	3	3	3	2	-	-	-	-	-	-	3	3	3	-
CO5	3	3	2	3	3	-	-	-	-	-	-	3	3	3	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Exam (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	15	-	-	30	-
Understand	40	20	45	10	10	50	10
Apply	-	80	-	90	90	20	90
Analyse	-	-	-	-	-	-	-
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV E34 – System On Chip								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

System Architecture* Components of The System – Processor Architectures – Memory and Addressing – System Level Interconnection – SoC Design Requirements and Specifications, Area-Time-Power Tradeoff In Processor Design.	[6]
Processor Selection for SOC* Soft Processors, Processor Core Selection, Instruction Set, Branches, Interrupts and Exceptions. Elements In Instruction Handling – Minimizing Pipeline Delays – Robust Processors.	[6]
Memory Design* SoC External Memory, SoC Internal Memory, Scratch Pads and Cache Memory – Cache Organization- Split I and D Caches – Multilevel Caches – SoC Memory Systems – Simple Processor/ Memory Interaction.	[6]
Interconnect Architectures and SOC customization* Bus Architectures – AMBA, Core Connect – Processor Customization Approaches – Reconfigurable Technologies – FPGA Based Design – Architecture of FPGA.	[6]
FPGA based Embedded Processor* Hardware Software Task Partitioning – FPGA Fabric Immersed Processors – Soft Processors and Hard Processors – Tool Flow for Hardware/Software Co-Design – Types of On-Chip Interfaces – Wishbone Interface, Avalon Switch Matrix, OPB Bus Interface.	[6]
Practical: 1. Study of RISC v and ARM Cortex-M1 2. Implementation of RISC-V-Processor on FPGA 3. Implementation of ARM Cortex M IP in FPGA 4. Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado Design Suite 5. Develop a system for temperature monitoring application **Tools used: Xilinx VIVADO**	[30]
Total Hours: (Lecture - 30; Practical - 30)	**60**
Text Book(s):	
1. Michael J.Flynn and Wayne Luk, “Computer system design system on Chip”, Wiley India Pvt. Ltd, 2011.	
2. Steve Furber, “ARM system on Chip Architecture “, Pearson, 2nd Edition, 2015.	
Reference(s):	
1. Veena S.Chakravarthi, ‘A Practical Approach to VLSI System On Chip Design’, Springer, 2020.	
2. Rainer Leupers, Olivier Temam, ‘Processor and System on Chip Simulation’, Springer, 2010.	
3. Sudeep Pasricha and NikilDutt,” On-Chip Communication Architecture System on Chip Interconnect”, Elsevier, 2008.	
4. https://www.btechguru.com/engineering-videos--electrical-engineering--circuit-theory--system-on-chip-(soc)-video-lecture--1790--4--21.html	

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**System Architecture**	
1.1	Components of the system	1
1.2	Processor architectures	1
1.3	Memory and addressing	1
1.4	System level interconnection	1
1.5	SoC design requirements and specifications	1
1.6	Area-time-power tradeoff in processor design	1
2.0	**Processor Selection for SOC**	
2.1	Soft processors, processor core selection	1
2.2	Instruction set, branches	1
2.3	Interrupts and exceptions	1
2.4	Elements in instruction handling	1
2.5	Minimizing pipeline delays	1
2.6	Robust processors	1
3.0	**Memory Design**	
3.1	SoC external memory, SoC internal memory	1
3.2	Scratch pads and cache memory	1
3.3	cache organization	1
3.4	Split I- and D caches, multilevel caches	1
3.5	SoC memory systems	1
3.6	Simple processor/ Memory interaction	1
4.0	**Interconnect Architectures and SOC Customization**	
4.1	Bus architectures	1
4.2	AMBA, Core Connect	1
4.3	Processor customization approaches	1
4.4	Reconfigurable technologies	1
4.5	FPGA based design	1
4.6	Architecture of FPGA	1
5.0	**FPGA based Embedded Processor**	
5.1	Hardware software task partitioning	1
5.2	FPGA fabric Immersed Processors	1
5.3	Soft Processors and Hard Processors	1
5.4	Tool flow for Hardware/Software Co-design	1
5.5	Types of On-chip interfaces – Wishbone interface	1
5.6	Avalon Switch Matrix, OPB Bus Interface	1

Course Designer(s)

1. Dr.S.Gomathi - gomathi@ksrct.ac.in

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60 EV E35	Mixed Signal Design	Category	L	T	P	Credit
		PE	2	0	2	3

Objectives

- To explore the types of filters for VLSI circuits.
- To learn the different techniques of ADC and DAC for mixed-signal circuits.
- To discuss the different DAC techniques for mixed-signal circuits.
- To interpret the concepts of sigma-delta converter for mixed-signal circuits.
- To study the design methodologies and EDA tools for mixed-signal VLSI circuits

Course Outcomes

On the successful completion of the course, students will be able to		
CO1	Describe the concept of different filter for VLSI circuit design	Understand
CO2	Explain the function of continuous time filter in MOS technology for mixed signal circuits	Understand
CO3	Discuss DAC and ADC techniques for data conversions using CMOS technologies	Understand
CO4	Describe the concept of sigma delta converter method for VLSI circuits	Understand
CO5	Illustrate the basic syntax and extension logic used for HDL in analog and mixed signals	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	-	-	-	-	-	-	-	-	3	2	-
CO2	3	3	3	2	-	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	2	-	-	-	-	-	-	-	3	3	-
CO4	3	3	3	2	2	-	-	3	3	3	-	-	3	3	2
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				Model Examination (Marks)	End Sem Examination (Marks)	
	Test 1		Test 2				
	Theory	Lab	Theory	Lab	Lab	Theory	Lab
Remember	20	-	20	-	-	30	-
Understand	40	-	40	-	-	70	-
Apply	-	60	-	60	60	-	60
Analyse	-	40	-	40	40	-	40
Evaluate	-	-	-	-	-	-	-
Create	-	-	-	-	-	-	-
Total	60	100	60	100	100	100	100

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K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E35 - Mixed Signal Design

Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

Switched Capacitor Filters* Switched Capacitor Filters: Switched Capacitor Resistors - Amplifiers – Comparators - Sample & Hold Circuits – Integrator- Biquad	[6]
Continuous Time Filters* Introduction to Gm - C Filters - Bipolar Transconductors - CMOS Transconductors Using Triode Transistors, Active Transistors – Bicmos Transconductors – MOSFET C Filters - Tuning Circuitry - Dynamic Range Performance - Elementary Transconductors Building Block- First Order Filter.	[6]
Digital to Analog & Analog to Digital Converters* Non-Idealities In The DAC - Types Of DAC's: Current Switched, Resistive, Charge Redistribution (Capacitive), - Techniques for Improving Linearity - Analog to Digital Converters: Nonidealities - Types of ADC's, Two Step, Pipelined, Folding ADC's.	[6]
Sigma Delta Converters Over Sampled Converters - Over Sampling Without Noise & With Noise - Implementation Imperfections - First Order Modulator - Sigma Delta DAC & ADC's	[6]
Analog and Mixed Signal Extensions to HDL* Introduction - Language Design Objectives - Theory Of Differential Algebraic Equations - Tolerance Groups - Conservative Systems - Time And The Simulation Cycle - A/D and D/A Interaction - Quiescent Point - Frequency Domain Modeling and Examples- Mixed Signal Interaction.	[6]
Particle: 1. Create an inverting amplifier circuit using Op-Amp, adjust resistor values, measure input and output voltages, and analyze amplification characteristics and frequency response. 2. Using an Op-Amp, construct a comparator circuit, vary the input voltages, measure the output voltage, and experiment with various voltage levels to determine the circuit's response. 3. Analyse the performance characteristics of different transconductor implementations (bipolar, CMOS, BiCMOS). 4. Construct first-order Gm-C filters using transductors; apply input signals with varying amplitudes and frequencies; 5. Using a 741 operational amplifier, construct a 4-bit R/2R ladder DAC while evaluating monotonicity, resolution, accuracy, linear errors, and settling time. 6. Construct an ADC circuit to convert 2 bit digital input to analog output. 7. Construct a first-order ΣΔ modulator circuit using operational amplifiers and passive components. 8. Analyse the circuit's efficiency with respect to linearity, stability, and signal-to-noise ratio. 9. Simulate and measure the performance of a Sigma-Delta DAC and ADC system. 10.Implement analog circuits like amplifiers and filters using HDL and simulate their behavior	[30]
Total Hours : 30+30(Practical)	**60**

Text Book(s):	
1.	David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2016.
2.	Rudy van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer, 2014.
Reference(s):	
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2012.
2.	Michael D.Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition, Pearson Education, 2011.
3.	Antoniou, "Digital Filters Analysis and Design", Tata McGraw Hill, 2010.
4.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.

*SDG 9 - Sustainable industrialization and foster innovation

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Active Filters and Switched Capacitor Filters**	
1.1	Switched Capacitor Filters	1
1.2	Switched Capacitor Resistors	1
1.3	Amplifiers & Comparators	2
1.4	Sample & Hold Circuits, Integrator-Biquad	2
2	**Continuous Time Filters**	
2.1	Gm - C filters, Bipolar Transconductors	1
2.2	CMOS Transconductors using Triode Transistors,	1
2.3	BiCMOS Transconductors MOSFET C Filters	1
2.4	Tuning Circuitry	1
2.5	Dynamic Range Performance	1
2.6	Elementary Transconductor Building Block - First Order Filters.	1
3	**Digital to Analog & Analog to Digital Converters**	
3.1	Non-idealities in the DAC	1
3.2	Types of DAC's: Current Switched	1
3.3	Resistive, Charge Redistribution (capacitive)	1
3.5	Analog to Digital Converters: Quantization Errors	1
3.6	Nonidealities - Two Step, Pipelined, Folding ADC's.	2
4	**Sigma Delta Converters**	
4.1	Over Sampled Converters	1
4.2	Over Sampling without Noise and with Noise	1
4.3	Implementation Imperfections	1
4.4	First Order Modulator	1
4.5	Sigma Delta DAC & ADC's.	2
5	**Analog and Mixed Signal Extensions to HDL**	
5.1	Language design objectives	1
5.2	Theory of Differential Algebraic Equations	1
5.3	Conservative Systems	1
5.4	Time and the Simulation Cycle	1
5.5	A/D and D/A Interaction, Quiescent Point	1
5.6	Frequency Domain Modeling and Examples	1
Practical:		
1.	Create an inverting amplifier circuit using Op-Amp, adjust resistor values, measure input and output voltages, and analyze amplification characteristics and frequency response.	2
2.	Using an Op-Amp, construct a comparator circuit, vary the input voltages, measure the output voltage, and experiment with various voltage levels to determine the circuit's response.	2
3.	Analyse the performance characteristics of different transconductor implementations (bipolar, CMOS, BiCMOS).	2
4.	Construct first-order and second-order Gm-C filters using transductors; apply input signals with varying amplitudes and frequencies;	2
5.	Using a 741 operational amplifier, construct a 4-bit R/2R ladder DAC while evaluating monotonicity, resolution, accuracy, linear errors, and settling time.	2
6.	Construct an ADC circuit to convert 2 bit digital input to analog output.	4
7.	Construct a first-order ΣΔ modulator circuit using operational amplifiers and passive components.	4
8.	Analyse the circuit's efficiency with respect to linearity, stability, and signal-to-noise ratio.	4
9.	Simulate and measure the performance of a Sigma-Delta DAC and ADC system.	4
10.	Implement analog circuits like amplifiers and filters using HDL and simulate their behavior	4

Course Designer(s)

1. Ms.R.Ramya - rramya@ksrct.ac.in

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Chairman - Board of Studies
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60 EV E36	Artificial Intelligence	Category	L	T	P	Credit
		PE	2	0	2	3

Objectives

- To interpret the concepts of the agents and environments in AI
- To discuss the fundamentals of problem-solving
- To explore the knowledge and reasoning in propositional logic and first-order logic
- To apply the uncertain knowledge in solving AI problems
- To discuss the different forms of learning

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the agents and environments in AI.	Understand
CO2	Explain the concepts of intelligent agents and problem-solving aspects.	Understand
CO3	Analyse the knowledge of propositional logic and first order logic.	Analyse
CO4	Describe the uncertainty and probabilistic reasoning.	Apply
CO5	Summarize the types of learning methods and AI applications.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	2	2	-	-	-	-	-	-	-	3	2	-
CO2	3	3	2	2	2	-	-	-	-	-	-	-	3	2	-
CO3	3	2	2	2	2	-	-	-	-	-	-	-	3	2	-
CO4	3	2	2	2	2	-	-	-	-	-	-	-	3	2	-
CO5	3	3	2	2	3	-	-	-	-	-	-	-	3	2	-

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)				End Sem Examination (Marks)	
	Test 1		Test 2			
	Theory	Lab	Theory	Lab	Theory	Lab
Remember	20	-	20	-	30	-
Understand	40	-	40	-	70	-
Apply	-	60	-	60	-	60
Analyse	-	40	-	40	-	40
Evaluate	-	-	-	-	-	-
Create	-	-	-	-	-	-
Total	60	100	60	100	100	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E36 - Artificial Intelligence

Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	2	0	2	60	3	50	50	100

Agents and Environments in AI* The Ethics and Risks of Developing Artificial Intelligence, AI: The Present and Future, Intelligent Agents: Agents and Environments, Good Behaviour: The Concept of Rationality, The Nature of Environments, The Structure of Agents	[6]
Search Algorithms* Solving Problems by Searching: Problem-Solving Agents, Uninformed Search Strategies, Informed (Heuristic) Search Strategies, Beyond Classical Search: Local Search Algorithms and Optimization Problems, Local Search in Continuous Spaces, Adversarial Search: Optimal Decisions in Game.	[6]
Knowledge and Reasoning* Logical Agents: Knowledge-based Agents, The Wumpus World, Agents based on Propositional Logic. First-Order Logic: Syntax and Semantics of First-Order Logic, Using First-Order Logic, Knowledge Engineering in First - Order Logic.	[6]
Uncertain Knowledge and Reasoning* Quantifying Uncertainty: Acting Under Uncertainty, Basic Probability Notation, Inference using Full Joint Distributions, Bayes' Rule and Its Use, Probabilistic Reasoning: Representing Knowledge in an Uncertain Domain, The Semantics of Bayesian Networks, Inference in Temporal Models, Hidden Markov Models.	[6]
Learning and Applications* Forms of Learning, Supervised Learning, Learning Decision Trees, Evaluating and Choosing the Best Hypothesis, Regression and Classification with Linear Models, Artificial Neural Networks, Nonparametric Models, Ensemble Learning, A Logical Formulation of Learning, Statistical Learning - Applications of Artificial Intelligence.	[6]
Practical: 1. Simulate Intelligent Agents and Analyse Their Behaviour. 2. Simulate Uninformed and Informed Search Strategies. 3. Simulate the Local Search Algorithms. 4. Simulate the Behaviour of Local Search Algorithms and Analyse Its Performance. 5. Write a Program to Generate the Output For A* Algorithm. 6. Write a Program to Show The Tic Tac Toe Game for 0 And X. 7. Simulate The Various Bayesian Parameters 8. Simulate Hidden Markov Models. 9. Simulate Supervised Learning for the Selected Problems-Based Regression. 10. Simulate Supervised Learning for The Selected Problems-Based Classification.	[30]
Total Hours: (Lecture - 30; Practical - 30)	**60**

Text Book(s):

1.	Melanie Mitchell, "Artificial Intelligence: A Guide for Thinking Humans", Farrar, Straus and Giroux Publisher, 2019
2.	Peter Norvig and Stuart Russel, "Artificial Intelligence: A Modern Approach", Pearson, 4th Edition, 2020.

Reference(s):

1.	Luger G., "Artificial Intelligence: Structures and Strategies for complex problem solving", 4th Edition, Pearson Education, 2016.
2.	Stuart Russell, "Human Compatible – Artificial Intelligence and the Problem of Control", Viking publisher, 2019.
3.	Nils J. Nilsson, "The Quest for Artificial Intelligence", Cambridge University Press, 2009.
4.	Nptel course, "Artificial Intelligence", https://nptel.ac.in/courses/106106126/

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1.0	**Agents and Environments in AI**	
1.1	The Ethics and Risks of Developing Artificial Intelligence	1
1.2	AI: The Present and Future, Intelligent Agents	1
1.3	Agents and Environments	1
1.4	Good Behaviour: The Concept of Rationality	1
1.5	The Nature of Environments, The Structure of Agents	2
2.0	**Search Algorithms**	
2.1	Solving Problems by Searching: Problem-Solving Agents	1
2.2	Uninformed Search Strategies, Informed (Heuristic) Search Strategies	1
2.3	Beyond Classical Search: Local Search Algorithms	1
2.4	Optimization Problems	1
2.5	Local Search in Continuous Spaces	1
2.6	Adversarial Search: Optimal Decisions in Game	1
3.0	**Knowledge, Reasoning**	
3.1	Logical Agents: Knowledge-Based Agents	1
3.2	The Wumpus World	1
3.3	Agents Based On Propositional Logic	1
3.4	First-Order Logic: Syntax and Semantics of First-Order Logic	1
3.5	Using First-Order Logic	1
3.6	Knowledge Engineering in First-Order Logic.	1
4.0	**Uncertain Knowledge and Reasoning**	
4.1	Quantifying Uncertainty: Acting Under Uncertainty	1
4.2	Basic Probability Notation, Inference Using Full Joint Distributions	1
4.3	Bayes' Rule And Its Use. Probabilistic Reasoning	1
4.4	Representing Knowledge in an Uncertain Domain,	1
4.5	The Semantics of Bayesian Networks, Inference in Temporal Models	1
4.6	Hidden Markov Models	1
5.0	**Learning and Applications**	
5.1	Forms of Learning, Supervised Learning	1
5.2	Learning Decision Trees, Evaluating and Choosing the Best Hypothesis	1
5.3	Regression and Classification with Linear Models	1
5.4	Artificial Neural Networks, Nonparametric Models	1
5.5	Ensemble Learning, A Logical Formulation of Learning	1
5.6	Statistical Learning - Applications of Artificial Intelligence	1
Practical:		
1.	Simulate Intelligent Agents and Analyse Their Behaviour.	2
2.	Simulate Uninformed and Informed Search Strategies.	2
3.	Simulate the Local Search Algorithms.	2
4.	Simulate the Behaviour of Local Search Algorithms and Analyse Its Performance.	2
5.	Write a Program to Generate the Output For A* Algorithm.	2
6.	Write a Program to Show The Tic Tac Toe Game for 0 And X.	4
7.	Simulate The Various Bayesian Parameters	4
8.	Simulate Hidden Markov Models.	4
9.	Simulate Supervised Learning for the Selected Problems-Based Regression.	4
10.	Simulate Supervised Learning for The Selected Problems-Based Classification.	4

Course Designer(s)

1. Ms.R.Ramya - rramya@ksrct.ac.in

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60 EV E41	Nanotechnology	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the fundamental types, characteristics, and fabrication techniques of nanotechnology and nanomaterials.
- To learn the preparation methods for nanomaterials and their applications in various fields.
- To explore the properties, types, and applications of carbon nanotubes in advanced technology.
- To analyze the interaction of light with nanomaterials and their implications in optics, photonics, and solar energy technologies.
- To comprehend the potential future applications of nanotechnology, including MEMS, nanomachines, and quantum computing.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Explain the fundamental concepts of nanotechnology, including its types, characterization techniques, and fabrication methods.	Understand
CO2	Apply various preparation methods like chemical vapor deposition and lithography to synthesize nanomaterials for practical applications.	Apply
CO3	Describe the properties, types, and applications of carbon nanotubes for advancements in nanotechnology.	Understand
CO4	Explain the interaction of light and nanomaterials and their applications in photonics, optics, and solar energy.	Understand
CO5	Apply the innovative solutions using nanotechnology for emerging applications in MEMS, nanodevices, and quantum computing.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	2	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO5	3	3	2	2	-	-	-	3	3	3	-	3	3	3	3

3 - Strong; 2 - Medium; 1 - Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	Test 1	Test 2	
Remember	10	15	20
Understand	70	85	60
Apply	20	-	20
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E41 - Nanotechnology

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Types and Characteristics of Nanotechnology* Background - Types of Nanotechnology and Nano - Machines-Top Down and Bottom-Up Techniques - Atomic Manipulation - Nanodots- Semi-Conductor Quantum Dots - Self-Assembly Monolayers- Simple Details of Characterization Tools- SEM, TEM, STM, AFM.	[9]
Nanomaterials* Nanomaterials - Preparation of Nanomaterials - Solid State Reaction Method - Chemical Vapor Deposition - SOL-GELS Techniques- Electrodeposition- Ball Milling- Lithography- Pulse Laser Deposition (PLD)- Applications of Nanomaterials	[9]
Carbon Tubes* New Forms of Carbon- Carbon tubes- Types of Nanotubes- Formation of Nanotubes- Assemblies- Purification of carbon Nanotubes- Properties of Nanotubes- Applications of Nanotubes.	[9]
Optics, Photonics and Solar Energy* Light and Nanotechnology- Interaction of light and Nanotechnology- Nanoholes and photons- Solar cells- Optically useful Nanostructured polymers- Photonic crystals.	[9]
Future Applications* MEMS- Nanomachines- Nanodevices- Quantum Computers - Opto-electronic Devices- Quantum Electronic devices- Environmental and Biological Applications.	[9]
Total Hours:	45

Text Book(s):

1.	Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse," Nanotechnology-Basic Science and Emerging Technologies", Overseas Press, 2002
2.	Mark Ratner and Daniel Ratner, "Nanotechnology-a Gentle Introduction to The Next Big Idea",Prentice Hall,2003

Reference(s):

1.	Rebecca L Johnson," Nanotechnology", Lerner Publications, 2003.
2.	Charles P. Poole Jr., "Introduction to Nanotechnogy",Chapman and Hall/CRS,2003.
3.	J P Colinge, FINFETs and other Multi-gate Transistors, Springer, Germany, 2010.
4.	B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, Pan Stanford Publisher, Singapore, 2012.

*SDG 9 – Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Types and Characteristics of Nanotechnology**	
1.1	Background	1
1.2	Types of Nanotechnology	1
1.3	Nano-machines	1
1.4	Top down and bottom-up techniques	1
1.5	Atomic manipulation-Nanodots,	1
1.6	Semi-conductor quantum dots	1
1.7	Self assembly monolayers	1
1.8	Simple details of characterization tools- SEM, TEM	1
1.9	STM, AFM	1
2.0	**Nanomaterials**	
2.1	Nanomaterials	1
2.2	Preparation of Nanomaterials	1
2.3	Solid state reaction method	1
2.4	Chemical Vapor Deposition	1
2.5	SOL-GELS techniques	1
2.6	Electrodeposition, ball milling	1
2.7	Lithography	1
2.8	Pulse Laser Deposition (PLD)	1
2.9	Applications of Nanotubes	1
3.0	**Carbon Tubes**	
3.1	New forms of carbon	1
3.2	Carbon tubes-types of Nanotubes	1
3.3	Formation of Nanotubes	2
3.4	Purification of carbon Nanotubes	2
3.5	Properties of Nanotubes	2
3.6	Applications of Nanotubes	1
4.0	**Optics, Photonics and Solar Energy**	
4.1	Light and Nanotechnology	1
4.2	Interaction of light and Nanotechnology	2
4.3	Nanoholes and photons	1
4.4	Solar cells	1
4.5	Optically useful Nanostructured polymers	2
4.6	Photonic crystals	2
5.0	**Future Applications**	
5.1	MEMS	1
5.2	Nanomachines	1
5.3	Nanodevices	1
5.4	Quantum Computers	1
5.5	Opto-electronic Devices	2
5.6	Quantum Electronic devices	2
5.7	Environmental and biological applications	1

Course Designer(s)

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60 EV E42	Analog IC Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the MOSFET device physics, small-signal and large-signal analysis techniques.
- To design and analyse fundamental analog building blocks, such as current mirrors, differential amplifiers, and operational amplifiers
- To understand the advanced circuit design techniques, including feedback amplifiers, frequency compensation, and noise analysis
- To understand the stability criteria of operational amplifiers and the factors that affect their stability.
- To understand the principles of switched-capacitor circuit design and phase-locked loop (PLL) techniques.

Pre-requisites

- Electronic Devices, Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Understand the MOSFET operation, small-signal and large-signal models.	Understand
CO2	Analyze the current mirrors, differential amplifiers, and operational amplifiers	Analyze
CO3	Analyze and optimize differential amplifiers for noise rejection and common-mode rejection	Analyze
CO4	Analyze multi-stage operational amplifiers, including frequency compensation techniques and power supply rejection	Analyze
CO5	Understand the switched-capacitor circuits and phase-locked loops, including design, analysis, and applications.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	3	-	3	-	-	3	3	3	-	3	3	3	3

3 - Strong; 2 - Medium; 1 – Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	30	30	40
Apply	10	10	20
Analyse	10	10	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E – Electronics Engineering(VLSI Design and Technology)

60 EV E42 - Analog IC Design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Single Stage Amplifiers and Differential Amplifiers* MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Second Order Effects, MOS Device Models, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage. Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS Loads, Gilbert Cell.	[9]
Current Mirrors, Amplifiers and Feedback* Cascode Current Mirrors, Active Current Mirrors, Large and Small Signal Analysis, Common Mode Properties. Feedback, Properties of Feedback Circuits, Types of Amplifiers, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise.	[9]
Frequency Response of Amplifiers and Noise* Miller Effect and Association of Poles with Nodes, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential pair. Noise Statistical Characteristics of Noise, Types of noise, Representation of noise in circuits, Noise in Single Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.	[9]
Operational Amplifier Stability and Frequency Compensation* One and Two Stage Op Amps, Gain Boosting, Common mode feedback, Slew rate, Power Supply Rejection. General Consideration of Stability and Frequency Compensation, Multipole System, Phase Margin, Frequency Compensation, Compensation of Two Stage Op Amps, Other Compensation Techniques.	[9]
Switched Capacitor Circuits and PLL* Sampling Switches, Switched Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback. Simple PLL, Charge Pump PLLs, Non-Ideal Effects in PLLs, Delay Locked Loops, Applications of PLL.	[9]
Total Hours:	45

Text Book(s):

1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001, 33rd re-print, 2016.
2.	Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, 5th Edition, Wiley, 2009.

Reference(s):

1.	Phillip Allen and Douglas Holmberg “CMOS Analog Circuit Design” Second Edition, Oxford University Press, 2004.
2.	D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, Wiley, 1997.
3.	R. Jacob Baker, “CMOS Circuit Design, Layout, and Simulation”, Third Edition, Wiley, 2010.
4.	https://link.springer.com/book/10.1007/978-90-481-3083-2

*SDG 4 - Quality Education

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Course Contents and Lecture Schedule		
S.No	**Topics**	**No.of Hours**
1.0	**Single Stage Amplifiers and Differential Amplifiers**	
1.1	MOSFET Structure, MOS Symbols, MOS I/V Characteristics	1
1.2	Second Order Effects	1
1.3	MOS Device Models	1
1.4	Common Source Stage, Source Follower	1
1.5	Common Gate Stage, Cascode Stage	1
1.6	Single Ended and Differential Operation	1
1.7	Basic Differential Pair, Common Mode Response	1
1.8	Differential Pair with MOS Loads	1
1.9	Gilbert Cell	1
2.0	**Current Mirrors, Amplifiers and Feedback**	
2.1	Cascode Current Mirrors	1
2.2	Active Current Mirrors	1
2.3	Large and Small Signal Analysis	1
2.4	Common Mode Properties	1
2.5	Feedback, Properties of Feedback Circuits	1
2.6	Types of Amplifiers	1
2.7	Feedback Topologies	1
2.8	Effect of Loading	1
2.9	Effect of Feedback on Noise	1
3.0	**Frequency Response of Amplifiers and Noise**	
3.1	Miller Effect and Association of Poles with Nodes	1
3.2	Common Source Stage, Source Followers	1
3.3	Common Gate Stage, Cascode Stage	1
3.4	Differential pair	1
3.5	Noise Statistical Characteristics of Noise	1
3.6	Types of noise, Representation of noise in circuits	1
3.7	Noise in Single Stage Amplifiers	1
3.8	Noise in Differential Pairs	1
3.9	Noise Bandwidth	1
4.0	**Operational Amplifier Stability and Frequency Compensation**	
4.1	One and Two Stage Op Amps	1
4.2	Gain Boosting	1
4.3	Common mode feedback	1
4.4	Slew rate, Power Supply Rejection	1
4.5	General Consideration of Stability and Frequency Compensation	1
4.6	Multipole System, Phase Margin	1
4.7	Frequency Compensation	1
4.8	Compensation of Two Stage Op Amps	1
4.9	Other Compensation Techniques	1
5.0	**Switched Capacitor Circuits and PLL**	
5.1	Sampling Switches	1
5.2	Switched Capacitor Amplifiers	1
5.3	Switched Capacitor Integrator	1
5.4	Switched Capacitor Common Mode Feedback	1
5.5	Simple PLL	1
5.6	Charge Pump PLLs	1
5.7	Non-Ideal Effects in PLLs	1
5.8	Delay Locked Loops	1
5.9	Applications of PLL	1

Course Designer

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60 EV E43	Memory Design and Testing	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To study the architectures for SRAM and DRAM
- To understand the concepts of various non-volatile memories.
- To illustrate the fault modelling and testing of memories for fault detection.
- To learn the radiation hardening process and issues for memory.
- To explore the knowledge of packaging technologies

Pre-requisites

- Digital System Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Analysis the different RAM architecture and interconnects.	Analyse
CO2	Analysis the different ROM architecture and interconnects.	Analyse
CO3	Describe about design and characterization technique	Understand
CO4	Describe the different memory testing and design for testability.	Understand
CO5	Identification of new developments in semiconductor memory design	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO2	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO3	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO4	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
CO5	3	3	3	-	3	-	-	-	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	30	50	60
Apply	-	-	-
Analyse	20	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E43 – Memory Design and Testing

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Random Access Memory Technologies* Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development - CMOS DRAMs DRAMs Cell Theory and Advanced Cell Strucutures - BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.	[9]
Non Volatile Memories * Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs - CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture - Non-volatile SRAM-Flash Memories (EPROMs or EEPROM) - Advanced Flash Memory Architecture.	[9]
Memory Fault Modeling, Testing, and Memory Design for Testability and Fault Tolerance* RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing Nonvolatile Memory Modeling and Testing - IDDQ Fault Modeling and Testing Application Specific Memory Testing. General Design for Testability Techniques – Ad Hoc Design Techniques, Structured Design Techniques – RAM Built-In Self – Test (BIST).	[9]
Reliability and Radiation Effects* General Reliability Issues-RAM Failure Modes and Mechanism - Non-volatile Memory Reliability Reliability Modeling and Failure Rate Prediction-Design for Reliability Reliability Test Structures Reliability screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP) - Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry - Water Level Radiation Testing and Test Structures.	[9]
Packaging Technologies* Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues - Memory Cards – High Density Memory Packaging Future Directions.	[9]
Total Hours:	45

Text Book(s):

1.	Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley2002.
2.	Ashok K.Sharma, Semiconductor Memories Technology, testing and reliability, Prentice hall of India Private Limited, New Delhi199.

Reference(s):

1.	Tegze P.Haraszti, “CMOS Memory Circuits”, Kluwer Academic publishers, 2001.
2.	Betty Prince, “Emerging Memories: Technologies and Trends”, Kluwer Academic publishers, 2002.
3.	AnjanGhosh, High Speed Semiconductor Devices, NPTELCourseware,2009.
4.	https://link.springer.com/book/10.1007/b101876

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Random Access Memory Technologies**	
1.1	Static Random Access Memories (SRAMs)	1
1.2	MOS SRAM Cell and Peripheral Circuit Operation-	1
1.3	Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-	1
1.4	Advanced SRAM Architectures and Technologies, Application Specific SRAMs	1
1.5	Dynamic Random Access Memories (DRAMs)	1
1.6	CMOS DRAMsDRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS,	1
1.7	DRAMs-Soft Error Failures in DRAMs	1
1.8	Advanced DRAM Designs and Architecture	1
1.9	Application, Specific DRAMs	1
2.0	**Non Volatile Memories**	
2.1	Masked Read-Only Memories (ROMs)-High Density ROMs	1
2.2	Programmable Read-Only Memories (PROMs)-BipolarPROMs	1
2.3	CMOS PROMs: Erasable (UV) Programmable Road-Only Memories (EPROMs)	2
2.4	Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs	1
2.5	Electrically Erasable PROMs (EEPROMs	1
2.6	EEPROM Technology And Arcitecture	1
2.7	Nonvolatile SRAM-Flash Memories, Advanced Flash Memory Architecture	2
3.0	**Memory Fault Modeling, Testing, and Memory Design for Testability and Fault Tolerance**	
3.1	RAM Fault Modeling, Electrical Testing	1
3.2	Pseudo Random Testing-Megabit DRAM Testing	1
3.3	Nonvolatile Memory Modeling and Testing	2
3.4	IDDQ Fault Modeling and Testing Application Specific Memory Testing	2
3.5	General Design for Testability Techniques – Ad Hoc Design Techniques	1
3.6	Structured Design Techniques	1
3.7	RAM Built-In Self – Test (BIST	1
4.0	**Reliability And Radiation Effects**	
4.1	General Reliability Issues-RAM Failure Modes and Mechanism	1
4.2	Nonvolatile Memory Reliability: Reliability Modeling and Failure Rate Prediction	1
4.3	Design for Reliability, Reliability Test Structures Reliability creening and Qualification	1
4.4	Radiation Effects-Single Event Phenomenon (SEP)	1
4.5	Radiation Hardening Techniques, Radiation Hardening Process	1
4.6	Radiation Hardened Memory Characteristics	1
4.7	Radiation Hardness Assurance and Testing	1
4.8	Radiation Dosimetry	1
4.9	Water Level Radiation Testing and Test Structures.	1
5.0	**Packaging Technologies**	
5.1	Random Access Memories (MRAMs)-Experimental Memory Devices	2
5.2	Memory Hybrids and MCMs (2D)	1
5.3	Memory Stacks and MCMs (3D)	1
5.4	Memory MCM Testing and Reliability Issues	2
5.5	Memory CardsHigh Density	1
5.6	Memory Packaging Future Directions	2

Course Designer(s)

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60 EV E44	Network on Chip	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the foundational principles of Network-on-Chip (NoC) architectures, including OSI layer adaptations, network topologies, and interconnection strategies.
- To Explore different switching techniques and packet formats used in advanced NoC communication, including wormhole and virtual channel (VC) router designs.
- To Examine routing strategies and flow control mechanisms to ensure efficient data transfer with QoS and congestion control within VLSI systems.
- To Investigate fault tolerance and reliability techniques in NoC, including fault-tolerant and adaptive routing algorithms for 2D and 3D mesh networks.
- To Apply security and verification methods to enhance the reliability and security of NoC infrastructure, including formal verification and fault-tolerant designs.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Identify the layers and rules of the OSI model as applied to Network-on-Chip architectures.	Understand
CO2	Describe various NoC topologies, switching techniques, and flow control protocols in the context of VLSI systems.	Understand
CO3	Classify routing strategies, including adaptive and multicast methods, used for both 2D and 3D mesh networks in NoC design.	Understand
CO4	Explain basic design principles for routers, including packet formats, FIFO, and GALS communication.	Understand
CO5	Discuss security and fault-tolerance measures in NoC design, such as formal verification and monitoring services.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	50	80
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E44 – Network on Chip

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Fundamentals of Network-on-Chip* Introduction to NoC – OSI layer rules in NoC – Interconnection Networks in Network-on-Chip -Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support	[9]
Advanced Communication and Routing Architectures in VLSI Systems* Switching Techniques and Packet Format – Asynchronous FIFO Design - GALS Style of Communication – Wormhole Router Architecture Design - VC Router Architecture Design – Adaptive Router Architecture Design.	[9]
Network Routing and Control Mechanisms* Packet Routing - Qos, Congestion Control and Flow Control –Router Design – Network Link Design – Efficient and Deadlock Free Tree-Based Multicast Routing Methods	[9]
Routing Strategies* Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms	[9]
Design Security and Reliability in NoC* Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on Chips.	[9]
Total Hours:	45

Text Book(s):

1.	Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R. Das" Networks-on - Chip "Architectures Holistic Design Exploration", Springer, 2010
2.	Giovanni De Micheli, Luca Benini, Davide Bertozzi, Networks on Chips: Technology and Tools, Morgan Kaufmann, 2006.

Reference(s):

1.	Fayez Gebali, Haytham El Miligi,, Hqhahed Watheq E1-Kharashi, "Networks-on-Chips theory and practice" CRC press, 2009.
2.	Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013.
3.	Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014.
4.	Santanu Kundu, SantanuChattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration", CRC Press, 2014

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Fundamentals of Network-on-Chip**	
1.1	Introduction to NoC	1
1.2	OSI layer rules in NoC	1
1.3	Interconnection Networks in Network-on-Chip	1
1.4	Network Topologies	1
1.5	Switching Techniques	1
1.6	Routing Strategies	1
1.7	Flow Control Protocol	1
1.8	Quality-of-Service Support	2
2.0	**Advanced Communication and Routing Architectures in VLSI Systems**	
2.1	Switching Techniques and Packet Format	2
2.2	Asynchronous FIFO Design	2
2.3	GALS Style of Communication	2
2.4	Wormhole Router Architecture Design	1
2.5	VC Router Architecture Design	1
2.6	Adaptive Router Architecture Design	1
3.0	**Network Routing and Control Mechanisms**	
3.1	Packet routing	2
3.2	Qos, congestion control	2
3.3	flow control	2
3.4	router design	1
3.5	network link design	1
3.6	Efficient and Deadlock Free Tree-Based Multicast Routing Methods	1
4.0	**Routing Strategies**	
4.1	Path-Based Multicast Routing for 2D Mesh Networks	2
4.2	Path-Based Multicast Routing for 3D Mesh Networks	2
4.3	Fault-Tolerant Routing Algorithms	2
4.4	Reliable Routing Algorithms	2
4.5	Adaptive Routing Algorithms	1
5.0	**Design Security and Reliability in NoC**	
5.1	Design-Security in Networks-on-Chips	2
5.2	Formal Verification of Communications in Networks-on Chips	2
5.3	Test Tolerance for Networks-on-Chip Infrastructures	2
5.4	Fault Tolerance for Networks-on-Chip Infrastructures	2
5.5	Monitoring Services for Networks-on Chips.	1

Course Designer(s)

1. Mr.D.Poornakumar - poornakumard@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV E45	IP based VLSI Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To Introduce the significance of Very-Large-Scale Integration in modern electronic systems and its impact on device miniaturization and performance enhancement.
- To Familiarize with integrated circuit (IC) manufacturing processes, focusing on CMOS technology and essential fabrication tools and software.
- To Provide foundational knowledge in combinational and sequential circuit design, including static and switch logic, clocking, and power optimization techniques.
- To Explore layout design, design rule checks (DRC), and the use of full-custom, semi-custom, and standard cell approaches for IC design.
- To understand the fundamentals of IP-based design, IP protection, and security techniques within the context of system-on-chip (SoC) development.

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Discuss the Role and Significance of VLSI in Modern Electronics	Understand
CO2	Describe IC Design Techniques and Layout Design Concepts	Understand
CO3	Illustrate Combinational and Sequential Logic Design for VLSI Circuits	Understand
CO4	Understand Floor Planning, Interconnect, and Advanced Architecture Design in VLSI	Understand
CO5	Discuss IP Design, Reuse, and Security in System-on-Chip (SoC) Development	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	-	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	50	80
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E45 – IP based VLSI design

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

VLSI Fabrication and Design Fundamentals* VLSI and its significance in modern electronics - IC Manufacturing Processes - CMOS Technology - IC Design Techniques: full-custom, semi-custom, and standard cell approaches - Layout Design Concepts: Design Rule Check (DRC), essential fabrication tools and software.	[9]
Combinational Circuits and Logic Design* Logic Gates - Static and Switch Logic: Basic concepts of static complementary logic gates and CMOS switch logic - Alternate Gate Design - Delay and Yield Considerations - IP-based Gate Design - Testing Strategies	[9]
Subsystem and Sequential Circuit Design* Sequential Circuits - Clocking and Power Optimization - Key Subsystems: multiplexers, decoders, basic datapath elements, and arithmetic circuits (adders and multipliers) - Memory Design - Reconfigurable Logic - Subsystem IP: Design and reuse of subsystems as intellectual property.	[9]
Floor Planning and Advanced Architecture Design* Floor Planning - Interconnect and Routing: Global interconnects, routing strategies, and off-chip connections (IO design, packaging, bonding). Advanced Architecture: HDL, pipelining techniques, high-level synthesis, and low-power methodologies in architecture design - GALS Systems - Architecture Testing	[9]
IP Design and Security* IP Reuse in SoC - IP Protection Techniques: constrained-based IP protection and watermarking techniques - Securing IP: Methods for securing IP during design, with a focus on legal and ethical considerations.	[9]
Total Hours:	45

Text Book(s):

1.	Khosrow Golshan, "SoC Design using IP Cores", Springer, 2007.
2.	Sudeep Pasricha, Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann, 2008.

Reference(s):

1.	Michael Keating, Pierre Bricaud, "Reuse Methodology Manual for System-on-a-Chip Designs", Springer, 2008.
2.	Farzad Nekoogar, Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall, 2003.
3.	Laung-Terng Wang, Charles Stroud, Nur A. Touba, "System-on-Chip Test Architectures: Nanometer Design for Testability", Morgan Kaufmann, 2007.
4.	Ricardo Reis, Marcelo Lubaszewski, Jochen A.G. Jess, "Design of Systems on a Chip: Design and Test", Springer, 2006.

*SDG 9 – Industry Innovation and Infrastructure

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**VLSI Fabrication and Design Fundamentals**	
1.1	VLSI and its significance in modern electronics	1
1.2	IC Manufacturing Processes	1
1.3	CMOS Technology	1
1.4	IC Design Techniques: full-custom	1
1.5	Semi-custom,	1
1.6	Standard cell approaches	1
1.7	Layout Design Concepts: Design Rule Check (DRC)	1
1.8	Essential fabrication tools and software.	2
2.0	**Combinational Circuits and Logic Design**	
2.1	Logic Gates	1
2.2	Basic concepts of static complementary logic gates	1
2.3	CMOS switch logic	1
2.4	Alternate Gate Design	1
2.5	Delay and Yield Considerations	1
2.6	IP-based Gate Design	2
2.7	Testing Strategies	2
3.0	**Subsystem and Sequential Circuit Design**	
3.1	Sequential Circuits	1
3.2	Clocking and Power Optimization	1
3.3	Key Subsystems: multiplexers	1
3.4	Decoders	1
3.5	Basic datapath elements	1
3.6	Arithmetic circuits (adders and multipliers) -	1
3.7	Memory Design	1
3.8	Reconfigurable Logic	1
3.9	Subsystem IP: Design and reuse of subsystems as intellectual property.	1
4.0	**Floor Planning and Advanced Architecture Design**	
4.1	Floor Planning	1
4.2	Interconnect and Routing: Global interconnects	1
4.3	Routing strategies	1
4.4	Off-chip connections (IO design, packaging, bonding).	1
4.5	Advanced Architecture: HDL	1
4.6	Pipelining techniques	1
4.7	High-level synthesis	1
4.8	Low-power methodologies in architecture design	1
4.9	GALS Systems - Architecture Testing	1
5.0	**IP Design and Security**	
5.1	IP Reuse in SoC	2
5.2	IP Protection Techniques: constrained-based IP protection	2
5.3	Watermarking techniques -	2
5.4	Securing IP: Methods for securing IP during design,	2
5.5	Focus on legal and ethical considerations.	1

Course Designer(s)

1. Mr.D.Poornakumar - poornakumard@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
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60 EV E46	Computer Vision: Algorithms and Applications	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To impart knowledge on image formation and processing
- To understand the computer and human vision systems
- To explore image processing techniques for computer vision applications
- To study the various concepts of deep learning for computer vision applications
- To learn object recognition methods and their applications

Pre-requisites

NIL

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Outline the various image interpolation techniques to enhance image quality during geometric transformations.	Remember
CO2	Describe the principles of computer and human vision systems.	Understand
CO3	Utilize the image processing techniques for computer vision.	Apply
CO4	Solve the various techniques and algorithms used in computer vision for a specific problem.	Apply
CO5	Apply object detection methods using the concept of computer vision.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	-
CO3	3	3	3	3	3	-	-	3	3	3	-	-	3	3	3
CO4	3	3	3	3	3	-	-	3	3	3	-	-	3	3	3
CO5	3	3	3	3	3	-	-	3	3	3	-	-	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	Test 1	Test 2	
Remember	20	15	30
Understand	40	30	60
Apply	-	15	10
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E – Electronics Engineering (VLSI Design and technology)

60 EV E46 - Computer Vision: Algorithms and Applications

Semester	Hours / Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VII	3	0	0	45	3	40	60	100

Image Formation and Processing Digital Image, Monochrome and Color Images, Image Brightness and Contrast, 2D, 3D, and 4D Images, Geometric Transformations - Image Interpolation, Nearest - Neighbor Interpolation, Bilinear Interpolation.	[9]
Machine Vision Computer and Human Vision Systems, The Human Eye, Evolution of Computer Vision, Camera Models - Machine Vision Lighting - Machine Vision Software - Machine Vision Automation - Integration of Machine Vision Components.	[9]
Image Processing for Computer Vision Applications Image Filtering - Bilateral Filter, Comparison of Filter Techniques - Image Segmentation - Motion Analysis: Differential Motion Analysis, Optical Flow, Analysis Based on Interest Points, Detection of Specific Motion Patterns, Video Tracking and Motion Estimation.	[9]
Deep Learning for Computer Vision* Deep Learning and Neural Networks for Vision - Convolutional Neural Networks (CNN) - Transfer Learning and FineTuning Pre - Trained Models - Performance Evaluation Metrics for Computer Vision Tasks.	[9]
Emerging Trends in Machine Vision**: Computer Vision and Industry 4.0 Applications: Object Detection and Semantic Segmentation - Variety of Approaches (YOLO) - Human Pose Estimation, Face ID, Face Detection and Recognition - Vehicle Vision System.	[9]
Total Hours:	**45**

Text Book(s):	
1.	Sheila Anand and L.Priya , “A Guide for Machine Vision in Quality Control”, Taylor & Francis Inc,Imprint CRC Press Inc, 2019.
2.	Richard Szeliski, “Computer Vision: Algorithms and Applications”, 2nd Edition, Springer-Texts in Computer Science, 2022.
Reference(s):	
1.	Rafael C. Gonzalez and Richard E. Woods, “Digital Image Processing”, Pearson Limited, 2018.
2.	Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing Analysis and Machine Vision”, 2nd Edition, Cengage learning, 2013.
3.	Joe Minichino Joseph Howse, “Learning OpenCV 3 Computer Vision with Python”, 2nd Edition, Packt Publishing Ltd, , 2015.
4.	D. A. Forsyth, J. Ponce, “Computer Vision: A Modern Approach”, 2nd Edition, Pearson Education, 2015.

*SDG 9 - Sustainable industrialization and foster innovation

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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Tiruchengode - 637 215

Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Image Formation and Processing**	
1.1	Digital Image, Monochrome and Color Images	1
1.2	Image Brightness and Contrast, 2D, 3D, and 4D Images	1
1.3	Geometric Transformations	1
1.4	Image Interpolation	1
1.5	Nearest-Neighbor Interpolation	1
1.6	Bilinear Interpolation.	1
2	**Machine Vision**	
2.1	Computer and Human Vision Systems	1
2.2	The Human Eye, Evolution of Computer Vision	1
2.3	Camera Models- Machine Vision Lighting	1
2.4	Machine Vision Software	1
2.5	Machine Vision Automation	1
2.6	Integration of Machine Vision Components	1
3	**Image Processing for Computer Vision Applications**	
3.1	Image Filtering-Bilateral Filter	1
3.2	Comparison of Filter Techniques, Image Segmentation	1
3.3	Motion Analysis: Differential Motion Analysis	1
3.4	Optical Flow, Analysis Based on Interest Points	1
3.5	Detection of Specific Motion Patterns	1
3.6	Video Tracking and Motion Estimation	1
4	**Deep Learning for Computer Vision**	
4.1	Deep Learning and Neural Networks for Vision	1
4.2	Convolutional Neural Networks (CNN)	1
4.3	CNN - Layers used to build ConvNets	1
4.4	Transfer Learning	1
4.5	Fine-Tuning Pre-Trained Models	1
4.6	Performance Evaluation Metrics for Computer Vision Tasks	1
5	**Emerging Trends in Machine Vision**	
5.1	Computer Vision and Industry 4.0, Applications: Object Detection	1
5.2	Semantic Segmentation, Variety of Approaches (YOLO)	1
5.3	Human Pose Estimation	1
5.4	Face ID, Face Detection	1
5.5	Face Recognition	1
5.6	Vehicle Vision System	1

Course Designer(s)

1. Ms.R.Ramya - rramya@ksrct.ac.in

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

60 EV E51	RTL Design and Synthesis	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To develop the combinational circuits using combinational logic design
- To develop the various sequential circuits using the concepts of sequential logic design
- To understand complex design and finite state machines
- To understand the concept of logic designs with delays and PLD-based designs
- To analyze the timing requirements of design

Pre-requisites

- Digital Logic Design

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Develop the various combinational circuits using combinational logic design	Apply
CO2	Develop the various sequential circuits using the concepts of sequential logic design	Apply
CO3	Interpret complex designs and improve the design performance of FSM	Understand
CO4	Illustrate the various digital logic designs with delays and PLD-based designs	Understand
CO5	Analyze the timing requirements of design, identifying violations and optimizing for speed, area, and power	Analyze

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	30
Understand	35	50	30
Apply	15	-	20
Analyse	-	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
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Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design & Technology)								
60 EV E51- RTL Design and Synthesis								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

Combinational Logic Design* Evolution of Logic Design, Integrated Circuit Design and Methodologies, Verilog HDL, Verilog Design Description, Verilog Arithmetic Operators, Verilog Logical Operators, Verilog Equality and Inequality Operators. Design of Multiplexers, Decoders, Encoders.	[9]
Sequential Logic Design* Sequential Design Guidelines - Use of Blocking Assignments, Nonblocking Assignments, Use of If-Else Versus Case Statements, Internally Generated Clocks, Use of Pipelining in Design. Design of JK Flip-flop, SR Flip-flop and T Flip-flop, D Flip-Flop, Synchronous and Asynchronous Reset, Synchronous Counters, Asynchronous Counter, Shift Registers, Memory Modules.	[9]
Complex Designs Using Verilog RTL* Design of ALU, Functions and Tasks, Parity Generators and Detectors, Barrel Shifters, Finite State Machines, Moore versus Mealy Machines, Finite State Machine (FSM), Encoding Styles, Sequence Detectors Using FSMs, Improving the Design Performance for FSMs.	[9]
Simulation Concepts with Delays and PLD-Based Designs* Blocking Assignments with Inter-assignment Delays and Intra-assignment Delays, Nonblocking Assignments with Inter-assignment Delays and Intra-assignment Delays. Implementation of PLA, PAL based design with delays. Introduction to PLD, FPGA as Programmable ASIC, FPGA Design Flow.	[9]
Timing Analysis* Timing Parameters, Positive and Negative Clock skew, Setup slack and Hold slack, Clock latency, Fixing Design Violations, Hold Violation and Setup Violations, Timing Exceptions in the Design, Area, Speed and Power requirements.	[9]
Total Hours:	45

Text Book(s):	
1.	Vaibbhav Taraate, Digital Logic Design Using Verilog Coding and RTL Synthesis, Springer, 2016
2.	Jan M.Rabaey, Digital Integrated Circuits: A design perspective, Pearson education, 2016
Reference(s):	
1.	Samir Palnitkar , Verilog HDL : A guide to digital design and synthesis, Prentice Hall PTR, Second edition,2003
2.	Sunggu lee, Advanced Digital Logic Design Using VHDL, State Machines, and Synthesis for FPGA's, CL- Engineering, 2005
3.	R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Third Edition, Wiley, 2010.
4.	https://link.springer.com/book/10.1007/978-981-16-3199-3

*SDG 4 - Quality Education

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Course Contents and Lecture Schedule		
S.No	**Topics**	**No.of Hours**
1.0	**Combinational Logic Design**	
1.1	Evolution of Logic Design	1
1.2	Integrated Circuit Design and Methodologies	1
1.3	Verilog HDL, Verilog Design Description	1
1.4	Verilog Arithmetic Operators	1
1.5	Verilog Logical Operators	1
1.6	Verilog Equality and Inequality Operators	1
1.7	Design of Multiplexers	1
1.8	Decoders	1
1.9	Encoders	1
2.0	**Sequential Logic Design**	
2.1	Sequential Design Guidelines - Use of Blocking Assignments	1
2.2	Nonblocking Assignments	1
2.3	Use of If-Else Versus Case Statements	1
2.4	Internally Generated Clocks	1
2.5	Use of Pipelining in Design	1
2.6	Design of JK Flip-flop, SR Flip-flop and T Flip-flop, D Flip-Flop	1
2.7	Synchronous and Asynchronous Reset	1
2.8	Synchronous Counters, Asynchronous Counter	1
2.9	Shift Registers, Memory Modules	1
3.0	**Complex Designs Using Verilog RTL**	
3.1	Design of ALU	1
3.2	Functions and Tasks	1
3.3	Parity Generators and Detectors	1
3.4	Barrel Shifters, Finite State Machines	1
3.5	Moore versus Mealy Machines	1
3.6	Finite State Machine (FSM)	1
3.7	Encoding Styles	1
3.8	Sequence Detectors Using FSMs	1
3.9	Improving the Design Performance for FSMs	1
4.0	**Simulation Concepts with Delays and PLD-Based Designs**	
4.1	Blocking Assignments with Inter-assignment Delays	1
4.2	Blocking Assignments with Intra-assignment Delays	1
4.3	Nonblocking Assignments with Inter-assignment Delays	1
4.4	Nonblocking Assignments with Intra-assignment Delays	1
4.5	Implementation of PLA, PAL based design with delays	2
4.6	Introduction to PLD	1
4.7	FPGA as Programmable ASIC	1
4.8	FPGA Design Flow	1
5.0	**Timing Analysis**	
5.1	Timing Parameters	1
5.2	Positive and Negative Clock skew	1
5.3	Setup slack and Hold slack	1
5.4	Clock latency	1
5.5	Fixing Design Violations	1
5.6	Hold Violation and Setup Violations	1
5.7	Timing Exceptions in the Design	1
5.8	Area, Speed and Power requirements	2

Course Designer

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Passed in BoS Meeting held on 13/06/2025

Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
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60 EV E52	Algorithms for VLSI Design Automation	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand fundamental graph structures such as complete, connected, and bipartite graphs, sub-graphs, and isomorphism.
- To explore and apply partitioning and floor planning algorithms and learn how these algorithms aid in creating optimized circuit layouts.
- To learn various placement and routing techniques and topological pin assignment to enhance physical design layout.
- To gain proficiency in clock tree topologies, buffer insertion and skew management for efficient clock distribution.
- To enhance skills in modelling and simulation, covering logic synthesis methods for optimized circuit performance.

Pre-requisites

- Digital Logic Design, Data Structures and Algorithms, Maths and Programming Skills, Circuits and Electrical and Electronic Fundamentals.

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Demonstrate the use of graph theory concepts in physical design problems, determine and analyse the computational complexity of physical design algorithms.	Apply
CO2	Describe the fundamentals of VLSI floor planning and partitioning, and explain the purpose and applications of each in the context of chip design.	Understand
CO3	Apply Concentric Circle Mapping and Topological Pin Assignment techniques to simplify placement for complex circuits, enhancing connectivity and reducing congestion.	Apply
CO4	Explain and apply various clock tree topologies to optimize clock distribution in VLSI circuits and evaluating their effectiveness in achieving robust and reliable clock signals.	Understand
CO5	Apply modelling and synthesis techniques, to simulate and verify digital designs to optimize circuit functionality and efficiency.	Apply

Mapping with Programme Outcomes

COs	POs											PSOs			
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	1	2	1	1	1	1	1	1	1	3	2	3
CO2	3	3	3	1	2	1	1	1	1	1	1	1	3	2	3
CO3	3	2	3	1	3	1	1	1	1	1	1	1	3	2	3
CO4	3	3	3	1	2	1	1	1	1	1	1	1	3	2	3
CO5	3	3	3	1	3	1	1	1	1	1	1	1	3	2	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	40	30	40
Apply	10	20	20
Analyse	-	-	20
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

Passed in BoS Meeting held on 13/06/2025
Approved in Academic Council Meeting held on 19/07/2025

Chairman - Board of Studies
Department of Electronics Engineering
(VLSI Design and Technology)
K. S. Rangasamy College of Technology
Tiruchengode - 637 215

Syllabus

K.S. Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering (VLSI Design and Technology)								
60 EV E52 – Algorithms for VLSI Design Automation								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

Graph Theory and Computational Complexity of Algorithms* Y Chart – Physical Design top-down flow – Review of Graph Theory: Complete Graph, Connected Graph, Sub Graph, Isomorphism, Bi partite graph tree, Big O-notation – Class P – Class NP -NP Hard -NP Complete.	[9]
Partitioning and Floor planning* Problem Formulation – Group Migration Algorithm – Kernighan Lin Simulated Annealing Based Partitioning – Stock Meyer Algorithm – Wong Liu Algorithm (Normalized Polish Expression), - Sequence Pair Technique.	[9]
Placement and Routing* Concentric Circle Mapping – Topological Pin Assignment – Power and Ground Routing – Wire Length Estimation Models for placement – Quadratic Placement – Grid Routing – Maze Routing – Global Routing – Detailed Routing – Dogleg Routing – Algorithms.	[9]
Clock Tree Topologies* Clocking Tree Topologies: H-tree, X-Tree – Method of Means and Medians (MMM) – recursive Geometric Matching – Elmore Delay Model to calculate skew – Buffer Insertion in clock trees – Exact zero skew clock routing algorithm – Clock Mesh Topologies – Uniform and non-uniform Mesh	[9]
Synthesis and Verification* Gate level modelling and simulation – Switch level modelling and Simulation – Combinational logic Synthesis – Binary Decision Diagrams – Two level Logic Synthesis – High Level Logic Synthesis	[9]
Total Hours:	45

Text Book(s):	
1.	Andrew B.Kahng, Jens Lienig, Igor L.Markov, Jin Hu, ”VLSI Physical Design: From Graph Partioning to Timing Closure, Springer International Publications, Second Edition,2022.
2.	Sabih H.Gerez, ”Algorithms for VLSI Design Automation”, John Wiley & Sons, Second Edition,1999.
References:	
1.	Sung Kyu LiM,” Practical Problems in VLSI Design Automation”, Springer International Publications, 2011.
2.	Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic Publishers”, Third Edition,1999.
3.	Sadiq M. Sait, Habib Youssef,” VLSI PHYSICAL DESIGN AUTOMATION: Theory and Practice” World Scientific Publishing,1999.
4.	Rajesh K.Maurya, Ganesh M.Mager,Swati R.Maurya, ”Graph Theory and Applications”, Technical Publications,2016.

*SD4: Quality Education

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Graph Theory and Computational Complexity of Algorithms**	
1.1	Y Chart	1
1.2	Physical Design top-down flow	1
1.3	Review of Graph Theory: Complete Graph	1
1.4	Review of Graph Theory: Complete Graph	1
1.5	Connected Graph, Sub Graph	1
1.6	Isomorphism, Bi partite graph tree	1
1.7	Big O-notation, Class P, Class NP	1
1.8	NP Hard, NP Complete	1
1.9	NP Hard, NP Complete	1
2.0	**Partitioning and Floor planning**	
2.1	Problem Formulation	1
2.2	Problem Formulation	1
2.3	Group Migration Algorithm	1
2.4	Group Migration Algorithm	1
2.5	Kernighan Lin Simulated Annealing Based Partitioning	1
2.6	Kernighan Lin Simulated Annealing Based Partitioning	1
2.7	Stock Meyer Algorithm	1
2.8	Wong Liu Algorithm (Normalized Polish Expression)	1
2.9	Sequence Pair Technique	1
3.0	**Placement and Routing**	
3.1	Concentric Circle Mapping	1
3.2	Topological Pin Assignment	1
3.3	Power and Ground Routing	1
3.4	Wire Length Estimation Models for placement	1
3.5	Quadratic Placement, Grid Routing	1
3.6	Maze Routing, Global Routing	1
3.7	Detailed Routing, Dogleg Routing	1
3.8	Algorithms	1
3.9	Algorithms	1
4.0	**Clock Tree Topologies**	
4.1	Clocking Tree Topologies: H-tree	1
4.2	Clocking Tree Topologies: X-Tree	1
4.3	Method of Means and Medians (MMM)	1
4.4	recursive Geometric Matching	1
4.5	Elmore Delay Model to calculate skew	1
4.6	Buffer Insertion in clock trees	1
4.7	Exact zero skew clock routing algorithm	1
4.8	Clock Mesh Topologies	1
4.9	Uniform and non-uniform Mesh	1
5.0	**Synthesis and Verification**	
5.1	Gate level modelling and simulation	1
5.2	Switch level modelling	1
5.3	Switch level Simulation	1
5.4	Combinational logic Synthesis	1
5.5	Binary Decision Diagrams	1
5.6	Binary Decision Diagrams	1
5.7	Two level Logic Synthesis	1
5.8	High Level Logic Synthesis	1
5.9	High Level Logic Synthesis	1

Course Designer(s)

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60 EV E53	DSP Structures for VLSI	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand the basic concepts and representations of DSP algorithms, including FIR and IIR filters.
- To learn iteration bounds to optimize DSP structures for low power and high performance.
- To design and implement fast convolution algorithms using advanced methodologies.
- To implement arithmetic strength reduction techniques for efficient filter design and parallel architectures.
- To implement pipelining and parallel processing methods in IIR filters, ensuring stability and throughput in real-time signal processing systems.

Pre-requisites

- Digital Signal Processing

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply filter realization techniques to design FIR and IIR filters for specific signal processing tasks.	Understand
CO2	Understand the data-flow graphs to compute iteration bounds and optimize FIR filter designs.	Apply
CO3	Apply Cook-Toom, Winograd, and iterated convolution methods to develop fast convolution algorithms.	Apply
CO4	Implement parallel architectures to enhance the performance and energy efficiency of FIR filters.	Apply
CO5	Implement pipelined and parallel processing techniques for IIR filters to enhance system throughput and efficiency.	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	2	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO3	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO4	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO5	3	3	2	2	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	Test 1	Test 2	
Remember	20	10	10
Understand	60	60	60
Apply	20	30	30
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022

B.E - Electronics Engineering (VLSI Design and Technology)

60 EV E53- DSP Structures for VLSI

Semester	Hours/Week			Total Hours	Credit	Maximum Marks		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

Digital Signal Processing Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG.	[9]
Iteration Bound Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm	[9]
Fast Convolution* Cook-Toom Algorithm- Modified Cook-Toom Algorithm- Winograd Algorithm-Iterated Convolution- Design of Fast Convolution Algorithm by Inspection.	[9]
Arithmetic Strength Reduction In Filters Parallel FIR filters-fast FIR algorithms-two parallel and three parallel- Parallel architectures for rank order filters -odd-even- merge-sort architecture-rank order filter architecture-parallel rank order filters-running order merge order sorter- low power rank order filter.	[9]
Pipelined and Parallel Recursive Filters Pipeline Interleaving in Digital Filters- Pipelining in First Order IIR Digital Filters- Pipelining in Higher-Order IIR Filters-Clustered Look Ahead and Stable Clustered Look Ahead-Parallel Processing for IIR Filters and Problems.	[9]
Total Hours:	45

Text Book(s):

1.	Keshab. K.Parhi, "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2014.
2.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Prentice Hall, Fourth Edition, 2015.

Reference(s):

1.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, 2014.
2.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, PHI, 2010.
3.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, McGraw-Hill, Fourth Edition, 2010.
4.	B. Venkataramani&M.Bhaskar, 'Digital Signal Processor Architecture, Programming and Application', 2 nd Edition, McGraw-Hill, 2014.

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**Digital Signal Processing**	
1.1	Linear system theory	1
1.2	Convolution	1
1.3	Correlation	1
1.4	DFT	1
1.5	FFT	1
1.6	Basic concepts in FIR filters and IIR filters	1
1.7	Filter realizations	1
1.8	Representations of DSP algorithms- block diagram	1
1.9	SFG, DFG	1
2.0	**Iteration Bound**	
2.1	Data-flow graph representations	2
2.2	Loop bound	2
2.3	Iteration bound algorithms for computing iteration bound	3
2.3	LPM algorithm	2
3.0	**Fast Convolution***	
3.1	Cook-Toom Algorithm	2
3.2	Modified Cook-Toom Algorithm	1
3.3	Winograd Algorithm	2
3.4	Iterated Convolution	2
3.5	Design of Fast Convolution Algorithm by Inspection.	2
4.0	**Arithmetic Strength Reduction In Filters**	
4.1	Parallel FIR filters	1
4.2	Fast FIR algorithms-two parallel and three parallel	1
4.3	Parallel architectures for rank order filters -odd-even	2
4.4	Merge-sort architecture	1
4.5	Rank order filter architecture	1
4.6	Parallel rank order filters	1
4.7	Running order merge order sorter	1
4.8	Low power rank order filter	1
5.0	**Pipelined and Parallel Recursive Filters**	
5.1	Pipeline Interleaving in Digital Filters	1
5.2	Pipelining in First Order IIR Digital Filters	2
5.3	Pipelining in Higher Order IIR Filters	1
5.4	Clustered Look ahead and Stable Clustered Look ahead	1
5.5	Parallel Processing for IIR Filters	2
5.6	Problems	2

Course Designer(s)

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60 EV E54	RFIC Design	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To understand Impedance Matching Techniques
- To analyze Amplifier Design Parameters
- To explore Active and Passive Mixer Designs
- To examine Oscillator Architectures
- To master PLL and Frequency Synthesizer Design

Pre-requisites

- Electronic Circuits

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Outline the principles of impedance matching in amplifiers	Understand
CO2	Illustrate the degenerated LNAs, Shunt feedback LNA, Noise cancelling LNAs	Understand
CO3	Explain the working of active and passive mixers	Apply
CO4	Classify the different types of oscillators and perform noise analysis	Analyze
CO5	Analyze the PLL and frequency synthesizer	Analyze

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO2	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO3	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO4	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
CO5	3	3	2	-	3	-	-	3	3	3	-	3	3	3	3
3 - Strong; 2 - Medium; 1 – Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	10	10	20
Understand	50	30	50
Apply	-	10	20
Analyse	-	10	10
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E - Electronics Engineering(VLSI Design and Technology)								
60 EV E54 - RFIC design								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

Impedance Matching in Amplifiers* Definition of 'Q', Series Parallel Transformations of Lossy Circuits, Impedance Matching Using 'L', 'Pi' and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers.	[9]
Amplifier Design* Noise Characteristics of MOS Devices, Resistive terminated CS and CG LNA, Inductive degenerated LNA, Shunt feedback LNA, Noise cancelling LNAs, Linearity Improvement Techniques.	[9]
Active and Passive Mixers* Passive Down-conversion Mixers, Current-Driven Passive Mixers, Active Down-conversion Mixers, Noise in Active Mixers, Active Mixers with Current-Source Helpers, Enhanced Transconductance, High IP_2, Low Flicker Noise, Up-conversion Mixers.	[9]
Oscillators* LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise.	[9]
PLL and Frequency Synthesizers* Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Integer-N Frequency Synthesizer, Fractional-N Frequency Synthesizer.	[9]
Total Hours:	45

Text Book(s):	
1.	B.Razavi , "RF Microelectronics" , Prentice-Hall, 2011
2.	Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press , 2003.
Reference(s):	
1.	Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001
2.	Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3.	https://ieeexplore.ieee.org/document/9100830
4.	Phillip E. Allen and Douglas R. Holberg- CMOS Analog Circuit Design Oxford University Press -3rd Ed., -2011.

*SDG 4 - Quality Education

Passed in BoS Meeting held on 13/06/2025
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Course Contents and Lecture Schedule

S.No	Topics	No.of Hours
1.0	**Impedance Matching in Amplifiers**	
1.1	Definition of 'Q'	1
1.2	Series Parallel Transformations of Lossy Circuits	1
1.3	Impedance Matching Using 'L', 'Pi' and T Networks	2
1.4	Integrated Inductors	1
1.5	Resistors	1
1.6	Capacitors	1
1.7	Tunable Inductors	1
1.8	Transformers	1
2.0	**Amplifier Design**	
2.1	Noise Characteristics of MOS Devices	2
2.2	Resistive terminated CS and CG LNA	2
2.3	Inductive degenerated LNA	1
2.4	Shunt feedback LNA	1
2.5	Noise cancelling LNAs	1
2.6	Linearity improvement techniques	2
3.0	**Active and Passive Mixers**	
3.1	Passive Down-conversion Mixers	1
3.2	Current-Driven Passive Mixers	1
3.3	Active Down-conversion Mixers	1
3.4	Noise in Active Mixers	1
3.5	Active Mixers with Current-Source Helpers	1
3.6	Enhanced Transconductance	1
3.7	High IP_2	1
3.8	Low Flicker Noise	1
3.9	Up-conversion Mixers	1
4.0	**Oscillators**	
4.1	LC Oscillators	1
4.2	Voltage Controlled Oscillators	1
4.3	Ring Oscillators	1
4.4	Delay Cells	1
4.5	Tuning Range in Ring Oscillators	1
4.6	Tuning in LC Oscillators	1
4.7	Tuning Sensitivity	1
4.8	Phase Noise in Oscillators	1
4.9	Sources of Phase Noise	1
5.0	**PLL and Frequency Synthesizers**	
5.1	Phase Detector/Charge Pump	1
5.2	Analog Phase Detectors	1
5.3	Digital Phase Detectors	1
5.4	Frequency Dividers	1
5.5	Loop Filter Design	1
5.6	Phase Locked Loops	1
5.7	Phase Noise in PLL, Loop Bandwidth	1
5.8	Integer-N Frequency Synthesizer	1
5.9	Fractional-N Frequency Synthesizer	1

Course Designer

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60 EV E55/60 EV L03	Micro Electro Mechanical Systems	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To introduce and provide a broad view of MEMS and micro systems
- To familiarize with the fundamentals of MEMS products, materials for microsystems
- To learn the microsystem fabrication process
- To know the various MEMS-specific design issues and constraints
- To familiarize with the application of MEMS sensors

Pre-requisites

- Nil

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Describe the basic principles of MEMS sensors and actuators.	Remember
CO2	Explain the various materials used for MEMS products.	Understand
CO3	Explain the fabrication process of MEMS devices.	Understand
CO4	Illustrate the design consideration, issues and constraints of basic MEMS sensors and actuators.	Understand
CO5	Extend the concepts of MEMS sensors in the diverse applications.	Understand

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO2	3	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO3	3	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO4	3	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO5	3	3	3	3	3	-	-	-	-	-	-	-	3	3	3

3 - Strong; 2 - Medium; 1 – Some

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	1	2	
Remember	30	30	40
Understand	30	30	60
Apply	-	-	-
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E. Electronics Engineering(VLSI Design and Technology)								
60 EV E55/60 EV L03 - Micro Electro Mechanical Systems								
Semester	**Hours/Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

MEMS* Scaling law – MEMS and Micro System Products – Microsystems and Microelectronics – Working Principle of Microsystems – Micro Actuation Techniques.	[9]
Materials for Microsystems* Substrate and Wafer – Single Crystal Silicon Wafer Formation – Ideal Substrates – Mechanical Properties – Silicon Compounds – $Si0_2$, SiC, Si_3N_4 and Polycrystalline Silicon – Silicon Piezo Resistors – Gallium Arsenide – Quartz – Piezoelectric Crystals – Polymers.	[9]
Micro System Fabrication Process* Photolithography – Doping Process – Ion Implantation – Diffusion – Oxidation – CVD – Physical Vapor Deposition – Deposition by Epitaxy – Etching Process – Wet and Dry Etching – Bulk Micromachining – Surface Micromachining.	[9]
Micro System Design* Design Considerations – Process Design – Mask Layout Design – Design Constraints – Selection of Materials – Manufacturing Process – Signal Transduction – Packaging Fundamentals – Packaging Techniques – Application of Micro System in Automotive Industry – Biomedical – Telecommunication – Carbon Nano Tubes.	[9]
Micro Sensors* Micro Sensors – Biomedical Sensors – Piezoresistive Sensors – Pressure Sensors – Thermal Sensors – Chemical Sensors – Optical Sensors – Micro Actuation – MEMS with Actuators.	[9]
Total Hours:	**45**

Text Book(s):	
1.	Tai-Ran Hus, "MEMS & Microsystems Design, Manufacture and Nano scale engineering", 2nd Edition, John Wiley & Sons, 2020.
2.	Julian W.Gardner, Vijay K.Varadan, Osama O.Awadel Karim, "Micro sensors MEMS and Smart Devices", John Wiley & Sons, 2013.
Reference(s):	
1.	Chang Liu, "Foundations of MEMS", 2nd Edition, Pearson Education Inc., 2012.
2.	Stephen D Senturia, "Microsystem Design"', Springer Publication, 2000.
3.	James J.Allen, "Micro Electro Mechanical System Design", CRC Press Publisher, 2005.
4.	Thomas M.Adams and Richard A.Layton, "Introductory MEMS: Fabrication and Application", Springer, 2010.

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of hours
1.0	**MEMS**	
1.1	Scaling Law	1
1.2	MEMS	1
1.3	MEMS Products	1
1.4	Micro System Products	1
1.5	Microsystems	1
1.6	Microelectronics	1
1.7	Working Principle of Microsystems	1
1.8	Micro Actuation	1
1.9	Micro Actuation Techniques	1
2.0	**Materials for Microsystems**	
2.1	Substrate and Wafer	1
2.2	Single Crystal Silicon Wafer Formation	1
2.3	Ideal Substrates	1
2.4	Mechanical Properties	1
2.5	Silicon Compounds	1
2.6	$Si0_2$, SiC, Si_3N_4 and Polycrystalline Silicon	1
2.7	Silicon Piezo Resistors – Gallium Arsenide	1
2.8	Quartz – Piezoelectric Crystals	1
2.9	Polymers	1
3.0	**Micro System Fabrication Process**	
3.1	Photolithography	1
3.2	Doping Process-Ion Implantation	1
3.3	Diffusion	1
3.4	Oxidation	1
3.5	CVD – Physical Vapor Deposition	1
3.6	Deposition by Epitaxy	1
3.7	Etching Process-Wet & Dry Etching	1
3.8	Bulk Micromachining	1
3.9	Surface Micromachining	1
4.0	**Micro System Design**	
4.1	Design Considerations- Process Design	1
4.2	Mask Layout Design – Design Constraints	1
4.3	Selection of Materials	1
4.4	Manufacturing Process - Signal Transduction	1
4.5	Packaging Fundamentals – Packaging Techniques	1
4.6	Application of Micro System In Automotive Industry	1
4.7	Biomedical – Aerospace	1
4.8	Telecommunication	1
4.9	Carbon Nano Tubes.	1
5.0	**Micro Sensors**	
5.1	Micro Sensors	1
5.2	Biomedical Sensors	1
5.3	Piezoresistive Sensors	1
5.4	Pressure Sensors	1
5.5	Thermal Sensors	1
5.6	Chemical Sensors	1
5.7	Optical Sensors	1
5.8	Micro Actuation	1
5.9	MEMS with Actuators	1

Course Designer(s)

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60 EV E56	Deep Learning	Category	L	T	P	Credit
		PE	3	0	0	3

Objectives

- To experiment the Convolutional Networks
- To utilize the Autoencoders
- To model the Deep Generative Models
- To model the Generative Adversarial Networks (GANs)
- To experiment with the Transformers architectures

Pre-requisites

- Machine Learning Techniques

Course Outcomes

On the successful completion of the course, students will be able to

CO1	Apply the Convolutional Networks in computer vision applications	Apply
CO2	Construct the different types of Autoencoders	Apply
CO3	Build the different boltzmann machines of the Deep Generative Models	Apply
CO4	Develop the different Generative Adversarial Networks (GANs) to increase the efficiency	Apply
CO5	Make use of various transformer architectures for text based applications	Apply

Mapping with Programme Outcomes

COs	POs												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	3	3	2	2	-	-	3	3	3	-	2	3	3	3
CO2	3	3	3	2	2	-	-	3	3	3	-	2	3	3	3
CO3	3	3	3	2	2	-	-	3	3	3	-	2	3	3	3
CO4	3	3	3	2	2	-	-	3	3	3	-	2	3	3	3
CO5	3	3	3	2	2	-	-	3	3	3	-	2	3	3	3
3 - Strong; 2 - Medium; 1 - Some															

Assessment Pattern

Bloom's Category	Continuous Assessment Tests (Marks)		End Sem Examination (Marks)
	Test 1	Test 2	
Remember	20	20	34
Understand	20	20	33
Apply	20	20	33
Analyse	-	-	-
Evaluate	-	-	-
Create	-	-	-
Total	60	60	100

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Syllabus

K.S.Rangasamy College of Technology – Autonomous R2022								
B.E – Electronics Engineering(VLSI Design and Technology)								
60 EV E56 – Deep Learning								
Semester	**Hours / Week**			**Total Hours**	**Credit**	**Maximum Marks**		
	L	T	P		C	CA	ES	Total
VIII	3	0	0	45	3	40	60	100

Convolutional Networks* The Convolution Operation - Motivation, Pooling - Convolution and Pooling as an Infinitely Strong Prior - Variants of the Basic Convolution Function - Structured Outputs - Data Types - Efficient Convolution Algorithms - Random or Unsupervised Features - Applications of DL in Computer Vision.	[9]
Autoencoders* Undercomplete Autoencoders - Stochastic Encoders and Decoders - Denoising Autoencoders - Learning Manifolds with Autoencoders - Contractive Autoencoders - Applications of Autoencoders	[9]
Deep Generative Models* Boltzmann Machines - Restricted Boltzmann Machines - Deep Belief Networks - Deep Boltzmann Machines - Boltzmann Machines for Real - Valued Data - Boltzmann Machines for Structured or Sequential Outputs - Directed Generative Nets	[9]
Generative Adversarial Networks (GANs)* Vanilla GAN - CycleGAN - StyleGAN - pixelRNN - DiscoGAN - lsGAN - EfficientNet-Compound Scaling - Focus on Efficiency - EfficientNet with Transformers - Pruning and Quantization Techniques	[9]
Transformers* Bidirectional Encoder Representations from Transformers (BERT - Generative Pre-trained Transformer 3 (GPT-3) - Text-to-Text Transfer Transformer (T5) - Generalized Autoregressive Pretraining for Language Understanding (XLNet)	[9]
Total Hours	**45**

Text Book(s):	
1.	Ian Goodfellow, Yoshua Bengio and Aaron Courville, “Deep Learning”, 2nd Edition, MIT Press, 2023.
2.	Nithin Buduma, Nikhil Buduma, Joe Papa, “Fundamentals of Deep Learning: Designing Next-Generation Machine Intelligence Algorithm”, 2nd Edition, O'Reilly Media, Inc., 2022.
Reference(s):	
1.	Rajalingappaa Shanmugamani , “Deep Learning for Computer Vision”, Packt Publishing, 2018
2.	Nikhil Ketkar, “Deep Learning with Python: A Hands-on Introduction”, Apress, 2017.
3.	https://deepmind.google/
4.	https://www.deeplearning.ai/

*SDG 9 – Industry Innovation and Infrastructure

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Course Contents and Lecture Schedule

S. No.	Topics	No. of Hours
1	**Convolutional Networks**	
1.1	The Convolution Operation	1
1.2	Motivation, Pooling, Convolution and Pooling as an Infinitely Strong Prior	1
1.3	Variants of the Basic Convolution Function, Structured Outputs	1
1.4	Data Types, Efficient Convolution Algorithms	1
1.5	Random or Unsupervised Features	1
1.6	Applications of DL in Computer Vision	1
2	**Autoencoders**	
2.1	Undercomplete Autoencoders	1
2.2	Stochastic Encoders and Decoders	1
2.3	Denoising Autoencoders	1
2.4	Learning Manifolds with Autoencoders	1
2.5	Contractive Autoencoders	1
2.6	Applications of Autoencoder	1
3	**Deep Generative Models**	
3.1	Boltzmann Machines, Restricted Boltzmann Machines	1
3.2	Deep Belief Networks	1
3.3	Deep Boltzmann Machines	1
3.4	Boltzmann Machines for Real-Valued Data	1
3.5	Boltzmann Machines for Structured or Sequential Outputs	1
3.6	Directed Generative Nets	1
4	**Generative Adversarial Networks (GANs)**	
4.1	Vanilla GAN,	1
4.2	CycleGAN, StyleGAN	1
4.3	PixelRNN, DiscoGAN,	1
4.4	lsGAN, EfficientNet - Compound Scaling, Focus	1
4.5	Efficiency, EfficientNet with Transformers	1
4.6	Pruning and Quantization Techniques	1
5	**Transformers**	
5.1	Bidirectional Encoder	1
5.2	Representations from Transformers (BERT)	1
5.3	Generative Pre-trained Transformer 3 (GPT-3)	1
5.4	Text-to-Text Transfer Transformer (T5)	1
5.5	Generalized Autoregressive Pretraining for Language Understanding (XLNet)	2

Course Designer(s)

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